

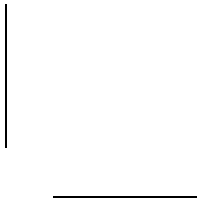
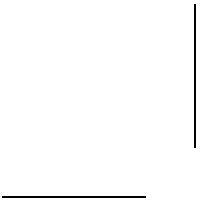


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*ST7050P*  
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***PC Card ATA and 68-Pin ATA***  
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***Interface Drive***  
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*Product Manual*  
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Publication Number: 36232-001 Rev. A

9 February 1994

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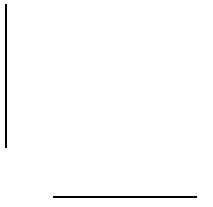
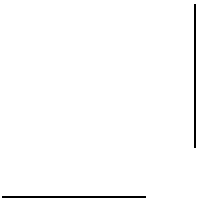
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## 1.0 Specification summary

### 1.1 Formatted capacity

Guaranteed Mbytes	42.7
Guaranteed sectors	83,520
Bytes per sector	512

### 1.2 Physical organization

Read/Write heads	2
Discs	1

### 1.3 Default logical geometry

Sectors per track	16
Read/Write heads	9
Cylinders	580

### 1.4 Functional specifications

Interfaces	PC Card ATA and 68-pin ATA
Recording method	RLL (1,7)
Recording density (BPI)	53,200
Flux density (FCI)	39,447
Track density (TPI)	2,748
Spindle speed (RPM)	3,545
Internal data transfer rate	up to 16 Mbits/sec (6 zones)—ZBR
I/O data transfer rate	up to 4 Mbytes/sec
Interleave	1:1
Cache buffer	32 Kbytes

## 1.5 Physical dimensions

Height (max)	0.413 inches (10.5 mm)
Width (max)	2.13 inches (54.1 mm)
Depth (max)	3.38 inches (85.8 mm)
Weight (max)	3.1 oz (88 g)

## 1.6 Seek time

Seek time is defined as the interval between the time the actuator begins to move and the time the head has settled over the target track. Seek times shown here do not include controller or host overhead. All measurements are taken at 5.0V at sea level and 25°C ambient temperature.

Track-to-track seek time is an average of all possible single-track seeks in both directions. Average seek time is measured by executing seek commands between random target tracks. Full-stroke seek time is one-half the time required for the drive to seek from track 0 to the highest-numbered track and back to track zero.

Track-to-track	
read (msec)	6
write (msec)	7
Average	
read (msec)	18
write (msec)	20
Full-stroke	
read (msec)	<28
write (msec)	<30
Average latency (msec)	8.46

## 1.7 Spinup times

Power-on to Ready (sec)	5 (typical)
Standby to Ready (sec)	2 (max)

## 1.8 Reliability

Nonrecoverable read errors	1 per $10^{13}$ bits read
Mean time between failures	300,000 power-on hours (nominal power, at sea level, 25°C ambient temperature)

## 1.9 Environment

### 1.9.1 Acoustics

Drive acoustics are measured as sound pressure 1 meter from the drive.

Idle mode (dBA, maximum)	24
Seek (dBA, maximum)	28

### 1.9.2 Ambient temperature

Operating	5°C to 55°C (41°F to 131°F)
Nonoperating	–40°C to 70°C (–40°F to 158°F)

### 1.9.3 Temperature gradient

Operating	30°C/hr max (54°F/hr), without condensation
Nonoperating	30°C/hr max (54°F/hr), without condensation

### 1.9.4 Relative humidity

Operating	8% to 80% noncondensing; 26°C (79°F) max wet bulb temperature
Nonoperating	8% to 90% noncondensing; 26°C (79°F) max wet bulb temperature

### 1.9.5 Altitude

Operating	–1,000 ft to 10,000 ft (–304.8 m to 3,048 m)
Nonoperating	–1,000 ft to 40,000 ft (–304.8 m to 12,192 m)

## 1.9.6 Shock

All shock specifications assume that the PC Card is mounted in an approved device with the shock applied directly to the card rails. The nonoperating specifications assume that the read/write heads are positioned in the shipping zone.

**Note.** At power-down and during Idle and Standby modes, the read/write heads automatically move to the shipping zone. The head and slider assembly park inside of the maximum data cylinder. When power is applied, the heads recalibrate to track 0.

### 1.9.6.1 Nonoperating shock

The following table shows the maximum shock the ST7050P can experience without incurring physical damage or degradation in performance when the drive is subsequently put into operation:

Shock duration	Maximum shock
< 0.15 msec	1,000 Gs
2.0 msec	200 Gs
11.0 msec	300 Gs

### 1.9.6.2 Operating shock

The ST7050P can withstand a 10-G shock of 11-msec duration without a reduction in drive performance. The drive can withstand a 15-G shock of 11-msec duration without damage, but performance may be degraded.

### 1.9.6.3 Rotational shock

The ST7050P can withstand a nonoperating rotational shock of 70,000 radians/sec<sup>2</sup> without incurring physical damage or degradation in performance when the drive is subsequently put into operation.

## 1.9.7 Vibration

All vibration specifications assume that the PC Card is mounted in an approved device with the shock applied directly to the card rails. The nonoperating specifications assume that the read/write heads are positioned in the shipping zone.

### 1.9.7.1 Nonoperating vibration

The ST7050P can withstand 22–500 Hz vibrations of 4.0 Gs (0 to peak) without incurring physical damage or degradation in performance when the drive is subsequently put into operation.

### 1.9.7.2 Operating vibration

The ST7050P can withstand 22–500 Hz vibrations of up to 0.5 Gs (0 to peak) without degraded drive performance. The drive can withstand 22–500 Hz vibrations of up to 0.75 Gs (0 to peak) without physical damage.

## 1.10 Power specifications

The ST7050P requires +5V (+ 5% – 10%) DC power supplied through the PCMCIA connector (see Section 3 for pin assignments).

### 1.10.1 Power-management mode descriptions

The ST7050P features four power-management modes: Active, Idle, Standby and Sleep. These modes are available to the drive in either PC Card ATA and in 68-pin ATA mode.

**Active mode.** In Active mode, the drive performs all normal disc activities, including reads, writes and seeks.

**Idle mode.** In Idle mode, the spindle remains up to speed, but the heads are parked away from the data zones for maximum data safety. The buffer remains enabled, and the drive accepts all commands. From Idle mode, the drive enters Active mode whenever disc access is necessary. At power-on, the drive sets the idle timer to 5 seconds (the drive enters Idle mode after 5 seconds of inactivity). In some computers, you can manually set the idle timer using the system setup utility.

**Standby mode.** In Standby mode, the buffer remains enabled, the heads are parked and the spindle is at rest. The drive accepts all commands and returns to Active mode whenever disc access is necessary. The drive enters Standby mode when the host sends a Standby Immediate command. If the host system has set the standby timer, the drive can also enter Standby mode automatically after the drive has been in Idle mode for a specifiable length of time. The standby timer delay is system-dependent and is usually set using the system setup utility.

**Sleep mode.** In sleep mode, the drive heads are parked and the spindle is at rest. The drive enters Sleep mode when a Sleep Immediate command has been received from the host. The drive leaves Sleep mode

when the host sends a Hard Reset or Soft Reset command. After the drive receives a soft reset, it exits Sleep mode with all current emulation and translation parameters intact.

**Idle and standby timers.** At power-on, the drive sets the default time delay for the idle timer to five seconds. In most systems, you can manually set this delay using the system setup utility. Each time the drive performs an Active function (read, write or seek), the idle timer is reinitialized and begins the countdown from the specified delay time to zero. If the idle timer reaches zero before any drive activity is required, the drive enters Idle mode.

If the host has set the standby timer, the drive begins the standby timer countdown as soon as it enters Idle mode. If the host has not set the standby timer, the drive remains in Idle mode. If the standby timer reaches zero before any drive activity is required, the drive enters Standby mode. In both Idle and Standby modes, the drive accepts all commands and returns to Active mode when disc access is necessary.

### 1.10.2 Power consumption

Power consumption by the ST7050P is shown in the table on page 7. Typical power measurements are based on an average of drives tested under nominal conditions using 5.0V input voltage at 25°C ambient temperature at sea level. Active mode power is measured with two spindle rotations between each operation and the drive in default logical geometry. Seek power is measured during one-third-stroke buffered seeks. Read/write power is measured with the heads on track.

Typical startup currents for the ST7050P are 0.45 amps (0.50 amps maximum). Transient state changes may cause current peaks above the maximum level.

Drive mode	Typical power consumption (watts RMS)
Active	
Seeking	1.2
Read/Write	1.2
Idle mode	0.43
Standby mode	0.10
Sleep mode	0.08

Figure 1 shows a typical current demand plot for the ST7050P.

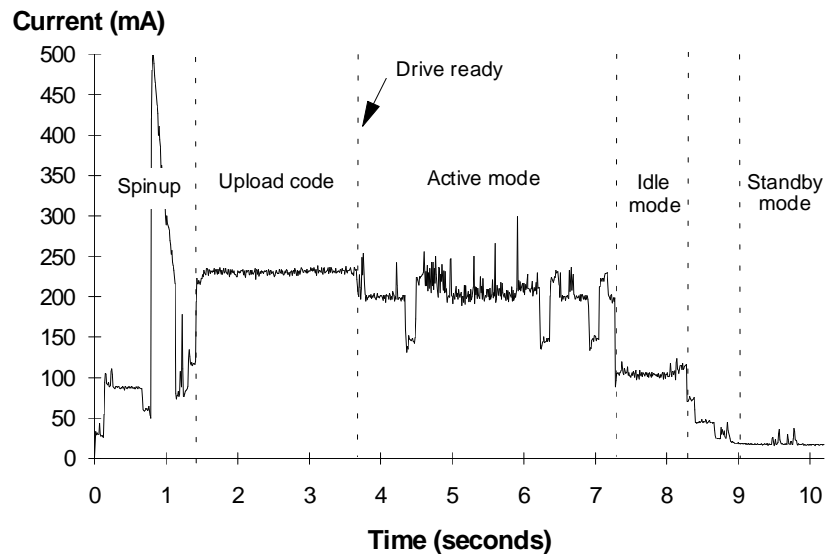


Figure 1. Startup and operations current profile for the ST7050P

### 1.10.3 Input power noise

The drive is expected to operate with a maximum of 150 mV peak-to-peak triangular wave injected noise at the power connector. The frequency is 10 Hz to 10 MHz with equivalent resistive loads. The voltage tolerance (including noise) is +5V (+ 5% – 10%).

### 1.11 UL/CSA certification

The ST7050P is recognized in accordance with UL 1950 and certified in accordance with CSA C22.2 (950-M-89) specifications. The drive meets all applicable sections of IEC 380, IEC 435, IEC 950, VDE 0806/08.81 and EN 60950 as tested by TUV-Rheinland, North America.

### 1.12 FCC verification

The ST7050P is intended to be contained solely within a personal computer or similar enclosure (not attached to an external device). As such, each drive is considered to be a subassembly even when it is individually marketed to the customer. As a subassembly, no Federal Communications Commission verification or certification of the device is required.

Seagate Technology, Inc. has tested this device in enclosures as described above to ensure that the total assembly (enclosure, disc drive, motherboard, power supply, etc.) does comply with the limits for a Class B computing device, pursuant to Subpart J, Part 15 of the FCC rules. Operation with noncertified assemblies is likely to result in interference to radio and television reception.

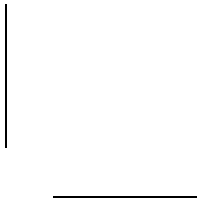
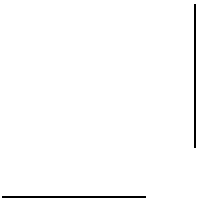
**Radio and television interference.** This equipment generates and uses radio frequency energy and if not installed and used in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception.

This equipment is designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television, which can be determined by turning the equipment on and off, you are encouraged to try one or more of the following corrective measures:

- Reorient the receiving antenna.
- Move the device to one side or the other of the radio or TV.
- Move the device farther away from the radio or TV.
- Plug the computer into a different outlet so that the receiver and computer are on different branch outlets.

If necessary you should consult your dealer or an experienced radio/television technician for additional suggestions. You may find helpful the following booklet prepared by the Federal Communications Commission: *How to Identify and Resolve Radio-Television Interference Problems*.

This booklet is available from the Superintendent of Documents, US Government Printing Office, Washington, DC 20402. Refer to publication number 004-000-00345-4.



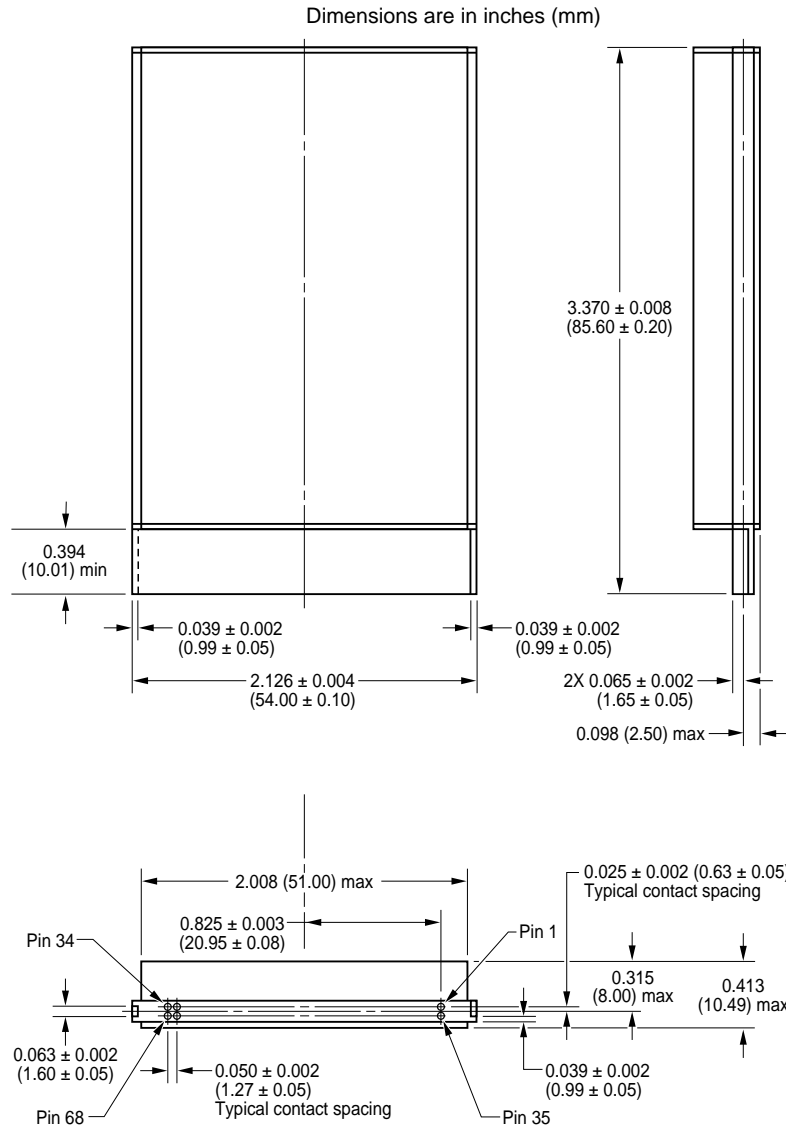
## **2.0 Drive handling and mounting**

### **2.1 Handling precautions**

The ST7050P, although shock-resistant, is susceptible to damage caused by rough handling, particularly when it is not mounted in a PCMCIA slot. Be careful not to drop the drive. Store the ST7050P in its protective case whenever it is not in use.

### **2.2 Mounting the ST7050P**

The ST7050P is designed to support the PCMCIA Type III standard for direct mounting. External dimensions for the ST7050P are shown in Figure 2 on page 12. You can mount and operate the ST7050P in any orientation. To mount the drive, simply insert it into a Type III PCMCIA slot. You may have to power down your computer before changing PC Cards. See your computer manual for details.



**Figure 2. ST7050P mounting dimensions**

### 3.0 PC Card ATA/68-pin ATA interface

The ST7050P supports the industry-standard ATA specification task-file interface and the PC Card ATA interface specification (Version 2.1).

Pin 9 is used to select either 68-pin ATA or PC Card ATA mode. If the OE $-$  signal is low during power-on reset, then the ST7050P configures itself as a 68-pin ATA drive. If the OE $-$  signal goes high within the first 100 msec after power-on, the ST7050P configures itself as a PC Card ATA drive. If the OE $-$  signal ever goes high after the first 100 msec following power-on, the drive enters an undefined state.

**Note.** To operate the drive only in 68-pin ATA mode, pin 9 of the host interface should be permanently connected to a DC ground.

#### 3.1 Features of the PC Card ATA interface

For a detailed description of the PC Card ATA interface, see the *PC Card ATA Specification*, available from:

PCMCIA  
1030G East Duane Avenue      Phone:  
Sunnyvale, CA 94086      (408) 720-0107

The ST7050P supports all standard PC Card ATA registers and bits except the audio, power-down, write protect, and battery voltage detection bits. The ST7050P does not currently support twin-card addressing.

##### 3.1.1 System compatibility

A large number of new PCMCIA host systems are currently entering the marketplace along with various implementations of the PC Card ATA interface. For a complete listing of systems that have been tested for compatibility with the ST7050P, contact Seagate technical support.

#### 3.2 Features of the 68-pin ATA interface

In general, the 68-pin ATA interface for the ST7050P uses the same basic ATA signals as Seagate's 3.5-inch and 1.8-inch AT drives. These signals are simply mapped to different pins. A detailed description of Seagate's implementation of the ATA interface is presented in the *Seagate ATA Interface Reference Manual*. Elements of the ATA interface that are unique to the ST7050P are summarized in the following sections of this manual.

In 68-pin ATA mode, the drive supports both 8-bit and 16-bit data transfer and has no DMA capability. All data transfers are completed through programmed I/O. The ST7050P does not currently support master-slave handshaking.

### 3.2.1 Remote LED

The drive indicates activity to the host through the DASP $\bar{}$  line on the ATA interface. This line can be connected to a drive status indicator driving an LED.

### 3.2.2 ATA bus signal levels

Signals sent by the drive have the following output characteristics at the drive connector:

Logic Low 0 to 0.4V                      Logic High 2.5 to 5.25V

Signals received by the drive must have the following input characteristics, measured at the drive connector:

Logic Low 0 to 0.8V                      Logic High 2.0 to 5.25V

## 3.3 Connector pin assignments and signals for the PC Card ATA and 68-pin ATA interfaces

The ST7050P uses a 68-pin connector with two rows of 34 pins. Figure 2 on page 12 shows the locations of pins 1, 34, 35 and 68. The ground pins are longer than the power pins, which in turn are longer than the signal pins. This allows the ST7050P to be hot plugged (inserted into a PCMCIA slot while the computer is powered up) when used with host systems that support hot plugging.

The table on pages 15 through 17 specifies pin assignments for the ST7050P in its three distinct interface modes. Signals used in PC Card ATA Memory mode and I/O mode are named in accordance with the PCMCIA *PC Card ATA Specification*. Signals used in 68-pin ATA mode are named for consistency with the draft proposed American National Standard ATA Interface Revision 4.0. For additional details on the ATA signals, see the *Seagate ATA Interface Reference Manual*.

In the following table NC indicates no connection. NU means that a pin is not used in that interface mode (and is in a high-impedance state). A signal name followed by a minus sign ( $\bar{}$ ) is an active-low signal. I/O signal direction is specified with respect to the host: I indicates to the host, O indicates from the host. Reserved pins and ground pins do not have direction.

Most signal names in the PC Card ATA column are used in both Memory mode and I/O mode. However, those marked with a superscript 1 are used only in Memory mode; those marked with a superscript 2 are used only in I/O mode.

Pin No.	I/O dir.	PC Card ATA: Memory mode <sup>1</sup> and I/O mode <sup>2</sup>	68-pin ATA mode
1	—	GND (ground)	GND (ground)
2	I/O	D3 (data bit 3)	DD3 (data bit 3)
3	I/O	D4 (data bit 4)	DD4 (data bit 4)
4	I/O	D5 (data bit 5)	DD5 (data bit 5)
5	I/O	D6 (data bit 6)	DD6 (data bit 6)
6	I/O	D7 (data bit 7)	DD7 (data bit 7)
7	I	CE1– (card enable 1)	CS1FX– (chip select 0)
8	I	A10 (address bus line 10)	NU
9	I	OE– (output enable)	ATA– (ATA mode select)
10	—	NC	NC
11	I	A9 (address bus line 9)	NU
12	I	A8 (address bus line 8)	NU
13	I	NC	NU
14	I	NC	NU
15	I	WE– (write enable)	NU
16	O	RDY/BSY– <sup>1</sup> (ready/busy) IREQ– <sup>2</sup> (interrupt request)	INTRQ (interrupt request)
17	—	VCC (5V power supply)	VCC (5V power supply)
18	—	NC	NC
19	—	NC	NC
20	—	NC	NC
21	—	NC	NC
22	I	A7 (address bus line 7)	NU

*continued*

*continued from previous page*

Pin No.	I/O dir.	PC Card ATA: Memory mode <sup>1</sup> and I/O mode <sup>2</sup>	68-pin ATA mode
23	I	A6 (address bus line 6)	NU
24	I	A5 (address bus line 5)	NU
25	I	A4 (address bus line 4)	NU
26	I	A3 (address bus line 3)	NU
27	I	A2 (address bus line 2)	DA2 (data address bit 2)
28	I	A1 (address bus line 1)	DA1 (data address bit 1)
29	I	A0 (address bus line 0)	DA0 (data address bit 0)
30	I/O	D0 (data bit 0)	DD0 (data bit 0)
31	I/O	D1 (data bit 1)	DD1 (data bit 1)
32	I/O	D2 (data bit 2)	DD2 (data bit 2)
33	O	WP <sup>1</sup> (write protect) IOIS16 <sup>-2</sup> (use 16 bit I/O)	IOCS16 <sup>-</sup> (use 16 bit I/O)
34	—	GND (ground)	GND (ground)
35	—	GND (ground)	GND (ground)
36	O	CD1 <sup>-</sup> (card detect 1)	CD1 <sup>-</sup> (card detect 1)
37	I/O	D11 (data bit 11)	DD11 (data bit 11)
38	I/O	D12 (data bit 12)	DD12 (data bit 12)
39	I/O	D13 (data bit 13)	DD13 (data bit 13)
40	I/O	D14 (data bit 14)	DD14 (data bit 14)
41	I/O	D15 (data bit 15)	DD15 (data bit 15)
42	I	CE2 <sup>-</sup> (card enable 2)	CS3FX <sup>-</sup> (chip select 1)
43	—	NC	NC
44	I	NU <sup>1</sup> IORD <sup>-2</sup> (I/O read)	DIOR <sup>-</sup> (I/O read)
45	I	NU <sup>1</sup> IOWR <sup>-2</sup> (I/O write)	DIOW <sup>-</sup> (I/O write)
46	—	NC	NC
47	—	NC	NC

Pin No.	I/O dir.	PC Card ATA: Memory mode <sup>1</sup> and I/O mode <sup>2</sup>	68-pin ATA mode
48	—	NC	NC
49	—	NC	NC
50	—	NC	NC
51	I	VCC (5V power supply)	VCC (5V power supply)
52	—	NC	NC
53	—	NC	NC
54	—	NC	NC
55	—	NC	NC
56	—	NC	NC
57	—	Reserved	Reserved
58	I	RESET (drive reset)	RESET– (drive reset)
59	O	WAIT– (extend bus cycle)	IORDY (I/O channel ready)
60	O	NU <sup>1</sup> INPACK– <sup>2</sup> (input acknowledge)	DMARQ (DMA request)
61	I	REG– (attribute memory)	DMACK– (DMA acknowledge)
62	0	NU	DASP– (drive active)
63	I/O	NU <sup>1</sup> STSCHG– <sup>2</sup> (status changed)	PDIAG– (passed diagnostics)
64	I/O	D8 (data bit 8)	DD8 (data bit 8)
65	I/O	D9 (data bit 9)	DD9 (data bit 9)
66	I/O	D10 (data bit 10)	DD10 (data bit 10)
67	—	CD2– (card detect 2)	CD2– (card detect 2)
68	I	GND (ground)	GND (ground)

### 3.4 PC Card ATA and 68-pin ATA interface commands

The following table lists ATA-standard and Seagate-specific drive commands that are supported by the ST7050P. For a detailed description of these commands, refer to the *Seagate ATA Interface Reference Manual*.

**Note.** The implementation of these commands is the same for a drive operating in a PC Card ATA environment or a drive operating in a 68-pin ATA environment.

Command name	Command code	Supported by ST7050P
<b>ATA-standard commands</b>		
Execute Drive Diagnostics	90H	Yes
Format Track	50H	Yes
Identify Drive	EC <sub>H</sub>	Yes
Initialize Drive Parameters	91H	Yes
NOP	00H	Yes
Read Buffer	E4 <sub>H</sub>	Yes
Read DMA (w/retry)	C8 <sub>H</sub>	No
Read DMA (no retry)	C9 <sub>H</sub>	No
Read Long (w/retry)	22 <sub>H</sub>	Yes
Read Long (no retry)	23 <sub>H</sub>	Yes
Read Multiple	C4 <sub>H</sub>	Yes
Read Sectors (w/retry)	20 <sub>H</sub>	Yes
Read Sectors (no retry)	21 <sub>H</sub>	Yes
Read Verify Sectors (w/retry)	40 <sub>H</sub>	Yes
Read Verify Sectors (no retry)	41 <sub>H</sub>	Yes
Recalibrate	1 <sub>xH</sub>	Yes
Seek	7 <sub>xH</sub>	Yes
Set Features	EF <sub>H</sub>	Yes
Set Multiple Mode	C6 <sub>H</sub>	Yes
Write Buffer	E8 <sub>H</sub>	Yes
Write DMA (w/retry)	CA <sub>H</sub>	No
Write DMA (no retry)	CB <sub>H</sub>	No
Write Long (w/retry)	32 <sub>H</sub>	Yes

Command name	Command code	Supported by ST7050P
Write Long (no retry)	33H	Yes
Write Multiple	C5H	Yes
Write Same	E9H	No
Write Sectors (w/retry)	30H	Yes
Write Sectors (no retry)	31H	Yes
Write Verify	3CH	No
<b>ATA-standard power-management commands</b>		
Check Power Mode	98H or E5H	Yes
Idle	97H or E3H	Yes
Idle Immediate	95H or E1H	Yes
Sleep	99H or E6H	Yes
Standby	96H or E2H	Yes
Standby Immediate	94H or E0H	Yes
<b>Seagate-specific power-management commands</b>		
Active and Set Idle Timer	FBH	Yes
Active Immediate	F9H	Yes
Check Idle Mode	FDH	Yes
Idle Immediate	F8H	Yes
Idle and Set Idle Timer	FAH	Yes

The following commands are specific to the ST7050P or contain drive-specific features.

### 3.4.1 Identify Drive command

The Identify Drive command (command code EC<sub>H</sub>) transfers information about the drive to the host following power up. When the command is issued, the drive sets BSY, prepares to transfer a single 512-byte block of data, sets DRQ and generates an interrupt. The host then reads the data from the drive. The data is organized as shown in the table below. All reserved bits or words should be set to zero.

The following table summarizes the information transferred by the Identify Drive command. Parameters listed with an “x” are drive specific or vary with the state of the drive. See Section 1 of this manual for default parameter settings for the ST7050P.

Word	Description	Contents
0	Configuration information: Bit 10: disc transfer $\leq$ 10 Mbits/sec Bit 6: fixed drive Bit 4: head switch time > 15 $\mu$ sec Bit 3: not MFM encoded Bit 1: hard sectored disc	045A <sub>H</sub>
1	Number of fixed cylinders (default logical emulation)	244 <sub>H</sub>
2	ATA reserved	0000 <sub>H</sub>
3	Number of heads (default)	0009 <sub>H</sub>
4	Number of unformatted bytes per track	8D90 <sub>H</sub>
5	Number of unformatted bytes per sector	248 <sub>H</sub>
6	Number of sectors per track (default logical emulation)	10 <sub>H</sub>
7–9	ATA reserved	0000 <sub>H</sub>
10–19	Serial Number: (20 ASCII characters, 0000 <sub>H</sub> = none)	ASCII
20	Controller type = dual-port multisector buffer with caching	0003 <sub>H</sub>
21	Buffer size (not supported)	0000 <sub>H</sub>
22	Number of ECC bytes available	000B <sub>H</sub>

<b>Word</b>	<b>Description</b>	<b>Contents</b>
23–26	Firmware revision (8 ASCII character string): <i>xx</i> = ROM ver., <i>ss</i> = RAM ver., <i>tt</i> = RAM ver.	<i>xx.ss.tt</i>
27–46	Drive model number: (40 ASCII characters, padded to end of string)	ST7050P
47	Maximum number of sectors transferred per interrupt during Read/Write Multiple commands.	0010 <sub>H</sub>
48	Double word I/O (not supported)	0000 <sub>H</sub>
49	LBA data transfer (supported) DMA data transfer (not supported)	0200 <sub>H</sub>
50	ATA reserved	0000 <sub>H</sub>
51	Minimum PIO data transfer cycle time	0000 <sub>H</sub>
52	Minimum DMA transfer cycle time (0 indicates DMA not supported)	0000 <sub>H</sub>
53	Validity of words 54–58 (1 indicates words may be valid)	0001 <sub>H</sub>
54	Number of cylinders (current emulation mode)	xxxx <sub>H</sub>
55	Number of heads (current emulation mode)	xxxx <sub>H</sub>
56	Number of sectors per track (current emulation mode)	xxxx <sub>H</sub>
57–58	Number of sectors (current emulation mode)	xxxx <sub>H</sub>
59	ATA reserved	0000 <sub>H</sub>
60–61	Total number of LBA user-addressable sectors	14640 <sub>H</sub>
62–127	ATA reserved	0000 <sub>H</sub>
128–159	Seagate reserved	xxxx <sub>H</sub>
160–255	ATA reserved	0000 <sub>H</sub>

### 3.4.2 Set Features command

This command controls the implementation of various features supported by the drive. When the drive receives this command, it sets BSY, checks the contents of the Features register, clears BSY, and generates an interrupt. If the value in the register does not represent a feature that the drive supports, the drive aborts the command. Power-on default settings are read look-ahead enabled, write cache disabled and 4 bytes of ECC. The acceptable values for the Features register are defined as follows:

- 02<sub>H</sub> Enables write cache feature
- 44<sub>H</sub> Eleven bytes of ECC apply on read long and write long commands.
- 55<sub>H</sub> Disables read look-ahead (read cache) feature
- 66<sub>H</sub> Disables reverting to power-on defaults feature
- 82<sub>H</sub> Disables write cache feature (*default*)
- AA<sub>H</sub> Enables read look-ahead (read cache) feature (*default*)
- BB<sub>H</sub> Four bytes of ECC apply on read long and write long commands (*default*).
- CC<sub>H</sub> Enables reverting to power-on defaults (*default*)

At power-on, or after a hardware reset, the default values of the features are as indicated above.

### 3.5 Card information structure

The card information structure (CIS) contains information used by the host in configuring socket services. This includes configuration for each of the four addressing modes supported by the ST7050P. This information is contained in a 256-byte segment of RAM, from 0 to 1FF<sub>H</sub>. The data is arranged in tuples, whose structure is described in the PCMCIA *PC Card ATA Specification*.

When the drive is powered up (for example, after being inserted into a PCMCIA slot), the drive sets up the CIS for the host to read, while asserting the BSY<sub>–</sub> signal. When the CIS is ready for the host to read, the drive asserts the RDY signal. The following table summarizes the tuples of the card information structure for the ST7050P.

<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
<b>Device Information Tuple</b>			
00	01	TUPLE CODE	CISTPL_DEVICE: Device Information Tuple
02	04	TUPLE LINK	Tuple has 4 bytes.
04	DF	DEVICE_INFO_1	I/O Device; WPS = 1; can always be written to; use extended speed byte.
06	42	DEVICE_INFO_2	Extended speed byte: speed (w/o wait) is 350 nsec.
08	01	—	Device Size: 2-Kbyte block; 1-Kbyte registers; 1-Kbyte buffer (Memory mode)
0A	FF	—	End of Device Information Tuple
<b>JEDEC Identifier Tuple</b>			
0C	18	TUPLE CODE	CISTPL_JEDEC: JEDEC Identifier Tuple
0E	02	TUPLE LINK	Tuple has 2 bytes.
10	DF	—	PCMCIA JEDEC Manufacturer ID Code
12	01	—	PCMCIA ATA – VCC only code
<b>Manufacturer ID Tuple</b>			
14	20	TUPLE CODE	CISTPL_MANFID: Manufacturer ID Tuple
16	04	TUPLE LINK	Tuple has 4 bytes.
18-1A	11, 01	—	PC Card manufacturer's ID for Seagate is 0111 <sub>H</sub> .
1C-1E	01, 00	—	Seagate product code = 0001 <sub>H</sub> .

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<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
<b>Product Information Tuple</b>			
20	15	TUPLE CODE	CISTPL_VERS_1: Product Information Tuple
22	23	TUPLE LINK	Tuple has 35 bytes.
24	04	TPLL1V1_MAJOR	Major version: always 04 <sub>H</sub> according to PCMCIA spec.
26	01	TPLL1V1_MINOR	Minor version: always 01 <sub>H</sub> for Release 2.0 and 2.01.
28-4C	53, 65, 61, 67, 61, 74, 65, 20, 54, 65, 63, 68, 6E, 6F, 6C, 6F, 67, 79, 00	TPLL1V1_INFO	Manufacturer information string = "Seagate Technology<00>".
4E-5C	53, 54, 37, 30, 35, 30, 50, 00	—	Product information string = "ST7050P<00>".
5E-64	41, 54, 41, 00	—	Additional information 1 = "ATA<00>".
66	00	—	Additional information 2 = null.
68	FF	—	End of Product Information Tuple.
<b>Function ID Tuple</b>			
6A	21	TUPLE CODE	CISTPL_FUNCID: Function ID Tuple
6C	02	TUPLE LINK	Tuple has 2 bytes.

<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
6E	04	—	PC Card function: fixed disc.
70	00	—	System initialization: no configuration necessary at power-on self-test.
<b>Function Extension Tuple (1)</b>			
72	22	TUPLE CODE	CISTPL_FUNCE: Function Extension Tuple (1)
74	02	TUPLE LINK	Tuple has 2 bytes.
76	01	—	Subfunction of disc function is interface type.
78	01	—	PC Card ATA interface.
<b>Function Extension Tuple (2)</b>			
7A	22	TUPLE CODE	CISTPL_FUNCE: Function Extension Tuple (2)
7C	03	TUPLE LINK	Tuple has 3 bytes.
7E	02	—	Subfunction of disc function is basic PC Card ATA option.
80	08	—	No Vpp required; rotating device; serial number is unique.
82	4E	—	Power management required; supports Idle, Standby, Sleep modes; include ports 3F7 <sub>H</sub> and 377 <sub>H</sub> ; no index; IOIS16 used in twin card.
<b>Configuration Tuple</b>			
84	1A	TUPLE CODE	CISTPL_CONFIG: Configuration Tuple
86	05	TUPLE LINK	Tuple has 5 bytes.

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<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
88	01	TPCC_SZ	Number of bytes in TPCC_RADR field = 1; base address is 2 bytes.
8A	03	TPCC_LAST	Last entry into configuration table is 3; last CIS index = 3.
8C	00	TPCC_RADR	Low byte of configuration register base address of 200 <sub>H</sub> .
8E	02	TPCC_RADR	High byte of configuration register base address of 200 <sub>H</sub> .
90	0F	TPCC_RMSK	CCR registers available (0–3); configuration option; configuration status; pin replacement, socket and copy.
<b>Configuration Entry Tuple</b>			
92	1B	TUPLE CODE	CISTPL_CE: Configuration Entry Tuple
94	06	TUPLE LINK	Tuple has 6 bytes.
96	C0	TPCE_INDEX	Configuration table index: Configuration 0 (memory); defaults for next memory entries.
98	C0	TPCE_IF	Interface description byte: Bits 0 to 3 = 0: Memory interface Bit 4 = 0: BVD not active Bit 5 = 0: Write Protect inactive Bit 6 = 1: RDY/BSY active Bit 7 = 1: Memory wait required
9A	A0	TPCE_FS	Feature selection byte: Bits 0, 1 = 0: Default Vcc Bit 2 to 4 = 0: No timing; no I/O; no IRQ specified Bits 5, 6 = 1: 2 bytes of TPCE_MS Bit 7 = 1: TPCE_MI to follow

<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
9C	08	TPCE_MS	Length of memory space is 8 * 256 bytes (low byte)
9E	00	TPCE_MS	Length of memory space is 8 * 256 bytes (high byte)
A0	00	TPCE_MI	Misc features: no twin cards; no audio; not read only; no power-down support; no extension.
<b>Configuration Entry Tuple</b>			
A2	1B	TUPLE CODE	CISTPL_CE: Configuration Entry Tuple
A4	08	TUPLE LINK	Tuple has 8 bytes.
A6	C1	TPCE_INDEX	Configuration Table Index: configuration 1 (block I/O); defaults for next I/O entries.
A8	C1	TPCE_IF	Interface description byte: Bits 0 to 3 = 1: I/O interface type Bit 4 = 0: BVD not active Bit 5 = 0: Write protect inactive Bit 6 = 1: RDY/BSY active Bit 7 = 1: Memory wait required
AA	98	TPCE_FS	Feature selection byte: Bits 0, 1 = 0: Default Vcc Bit 2 = 0: No timing specified Bit 3 = 1: I/O description to follow Bit 4 = 1: IRQ description to follow Bits 5, 6 = 0: No memory space Bit 7 = 1: TPCE_MI is specified
AC	64	TPCE_IO	I/O space required: Bits 0–4 = 4: Number of I/O address lines is 4. Bits 5, 6 = 1: Both 8-bit (byte) and 16-bit (word) access permitted. Bit 7 = 0: All I/O addresses are decoded.

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<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
AE	F0	TPCE_IR	IRQ description: card can share IRQ; both pulse and level; mask to follow.
B0	FF	TPCE_IR	IRQ description: any IRQ; 0–7 recommended.
B2	FF	TPCE_IR	IRQ description: any IRQ; 8–15 recommended.
B4	00	TPCE_MI	Misc. features: no twin cards; no audio; not read only; no power-down support; no extension.
<b>Configuration Entry Tuple</b>			
B6	1B	TUPLE CODE	CISTPL_CE: Configuration Entry Tuple
B8	0D	TUPLE LINK	Tuple has 13 bytes.
BA	82	TPCE_INDEX	Configuration table index: configuration 2 (I/O primary); interface byte to follow; defaults from previous I/O entry.
BC	C1	TPCE_IF	Interface description byte: Bits 0–3 = 1: I/O interface type Bit 4 = 0: BVD not active Bit 5 = 0: Write Protect inactive Bit 6 = 1: RDY/BSY active Bit 7 = 1: Memory wait required
BE	98	TPCE_FS	Feature Selection byte: Bits 0, 1 = 0: Default Vcc Bit 2 = 0: No timing specified Bit 3 = 1: I/O description to follow Bit 4 = 1: IRQ description to follow Bits 5, 6 = 0: No memory space Bit 7 = 1: TPCE_MI specified

<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
C0	EA	TPCE_IO	I/O Space Required: Bits 0–4 = 10: Number of I/O address lines = 10 Bits 5, 6 = 1: Both 8 bit (byte) and 16 bit (word) access permitted Bit 7 = 1: Decode range to follow
C2	61	TPCE_IO_RANGE	I/O ranges: Bits 0–4 = 1: 2 I/O ranges Bits 4, 5 = 10: 2-byte address Bits 6, 7 = 01: Address is 1 byte long.
C4	F0	TPCE_IO_RANGE1	I/O address range 1 begins at 1F0 <sub>H</sub> (low byte).
C6	01	TPCE_IO_RANGE1	I/O address range 1 begins at 1F0 <sub>H</sub> (high byte).
C8	07	TPCE_IO_RANGE1	The address is 8 bytes long (from 1F0 <sub>H</sub> to 1F7 <sub>H</sub> ).
CA	F6	TPCE_IO_RANGE2	I/O address range 2 begins at 3F6 <sub>H</sub> (low byte).
CC	03	TPCE_IO_RANGE2	I/O address range 2 begins at 3F6 <sub>H</sub> (high byte).
CE	01	TPCE_IO_RANGE2	The address is 2 bytes long (from 3F6 <sub>H</sub> to 3F7 <sub>H</sub> ).
D0	EE	TPCE_IR	IRQ description 1: card can share IRQ; both pulse and level; recommend IRQ14.
D2	00	TPCE_MI	Misc feature: no twin cards; no audio; not read only; no power-down support; no extension.

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<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
<b>Configuration Entry Tuple</b>			
D4	1B	TUPLE CODE	CISTPL_CE: Configuration Entry Tuple
D6	0D	TUPLE LINK	Tuple has 13 bytes.
D8	83	TPCE_INDEX	Configuration table index: configuration 3 (I/O secondary); interface byte to follow; defaults from first I/O entry.
DA	C1	TPCE_IF	Interface description byte: Bits 0–3 = 1: I/O interface type Bit 4 = 0: BVD not active Bit 5 = 0: Write protect inactive Bit 6 = 1: RDY/BSY active Bit 7 = 1: Memory wait required
DC	98	TPCE_FS	Feature selection byte: Bits 0, 1 = 0: Default Vcc Bit 2 = 0: No timing specified Bit 3 = 1: I/O description to follow Bit 4 = 1: IRQ description to follow Bits 5, 6 = 0: No memory space Bit 7 = 1 : TPCE_MI specified
DE	EA	TPCE_IO	I/O space required: Bits 0–4 = 10: Number of I/O address lines = 10. Bits 5, 6 = 1: Both 8-bit (byte) and 16-bit (word) access permitted. Bit 7 = 1: Decode range to follow
E0	61	TPCE_IO_RANGE	I/O ranges: Bits 0–4 = 1: 2 I/O ranges Bits 4, 5 = 10: 2-byte address Bits 6, 7 = 01: Address is 1 byte long.
E2	70	TPCE_IO_RANGE1	I/O address range 1 begins at 170 <sub>H</sub> (low byte).

<b>ST7050P Card Information Structure</b>			
<b>Offset (hex)</b>	<b>Value (hex)</b>	<b>Code</b>	<b>Description</b>
E4	01	TPCE_IO_RANGE1	I/O address range 1 begins at 170 <sub>H</sub> (high byte).
E6	07	TPCE_IO_RANGE1	The address is 8 bytes long (from 170 <sub>H</sub> to 177 <sub>H</sub> ).
E8	76	TPCE_IO_RANGE2	I/O address range 2 begins at 376 <sub>H</sub> (low byte).
EA	03	TPCE_IO_RANGE2	I/O address range 2 begins at 376 <sub>H</sub> (high byte).
EC	01	TPCE_IO_RANGE2	The address is 2 bytes long (from 376 <sub>H</sub> to 377 <sub>H</sub> ).
EE	EE	TPCE_IR	IRQ description 1: card can share IRQ, both pulse and level; recommend IRQ14.
F0	00	TPCE_MI	Misc. features: no twin cards; no audio; not read only; no power-down support; no extension.
<b>No Long-Link Tuple</b>			
F2	14	TUPLE CODE	CISTPL_NO_LINK: No Long-Link Tuple.
F4	00	TUPLE LINK	Null, must be 0
F6	FF	TUPLE_END	<b>CISTPL_END: End of CIS.</b>

### 3.6 Card-configuration registers

The host uses four card-configuration registers to configure the PC Card. After you insert the card into the host, the host reads the CIS to determine the configuration and options that the drive interface supports. The Configuration Tuple specifies the base address of the CCR and indicates whether all four CCRs are supported. The ST7050P supports all four registers, but not all bits within each register. In the tables below, NS indicates that the bit is not supported by the ST7050P and should be assigned a value of 0.

### 3.6.1 Configuration Option register

The host can read this register to obtain current setup information, and can write to this register to reset the drive and to select interrupt and access modes. The bits in this register are shown below.

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	LevIREQ	Configuration Index					

**SRESET:** The host causes the drive to enter a reset state by writing a one (1) to this bit. This has the same effect as asserting the RESET signal on the bus. The host must write a zero (0) to cause the drive to exit the reset state. After being placed in a reset state, the drive will be reconfigured as if it was just powered on.

**LevIREQ:** The host writes to this bit to select Level mode interrupts or Pulse mode. In Level mode, the interrupt line is held low until the host services it. In Pulse mode, the line is held low for at least 0.5  $\mu$ sec after an interrupt occurs. The default state for the ST7050P is Pulse mode.

**Configuration Index:** The host writes to this field an index number corresponding to the CIS Configuration Entry Tuple for the desired access mode to be used by the PC Card. The index modes are as follows:

- 00<sub>H</sub>: Memory mode with linear addressing (default mode)
- 01<sub>H</sub>: I/O mode with linear addressing
- 02<sub>H</sub>: I/O mode with primary ATA addressing
- 03<sub>H</sub>: I/O mode with secondary ATA addressing

### 3.6.2 Configuration and Status register

The host can read this register to obtain drive status information and can write to it to set drive configuration parameters. The bits for this register are shown in the following table.

D7	D6	D5	D4	D3	D2	D1	D0
Changed	SigChg	IOis8	Reserved	Audio (NS)	PwrDwn (NS)	Intr	Reserved

**Changed:** When set to 1, this bit indicates that the CRdy/Bsy or CWProt bits in the Pin Replacement register are set to one (see following section).

**SigChg:** The host uses this bit to enable or disable a state-change "signal" from the Status register. When this bit is set and the card is configured for I/O mode, the Changed bit controls pin 63 (STSCHG-) on

the interface. If this is not desired, the host should set this bit to 0, so that the STSCHG– signal is held high regardless of which mode the drive is in. The default value for this bit is 0.

**IOis8:** The host sets this bit equal to 1 if it can support only 8-bit data transfers. The default value for this bit is 0.

**Audio:** Not supported by the ST7050P

**PwrDwn:** Not supported by the ST7050P

**Intr:** This read-only bit indicates the internal state of the Interrupt Request signal in PC Card ATA I/O mode.

### 3.6.3 Pin Replacement register

This register provides interface signal information that may be necessary for drive operation in Memory mode. The bits in this register are shown in the following table.

D7	D6	D5	D4	D3	D2	D1	D0
CBVD1 (NS)	CBVD2 (NS)	CRdy/ Bsy	CWProt (NS)	RBVD1 (NS)	RBVD2 (NS)	RRdy/ Bsy	RWProt (NS)

**CBVD1, CBVD2, RBVD1, RBVD2:** Battery voltage detect bits (not supported by the ST7050P).

**CRdy/Bsy:** This bit is set to 1 if the RDY/BSY signal (pin 16) changes state. The host may write to this bit for its own use.

**CWProt, RWProt:** Write protect bits (not supported by the ST7050P)

**RRdy/Bsy:** The host may read this bit to determine the internal state of the RDY/BSY signal. The host may also use this bit to determine the state of the PC Card when it is configured for I/O mode and pin 16 is used for the IREQ signal.

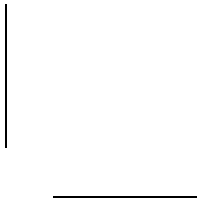
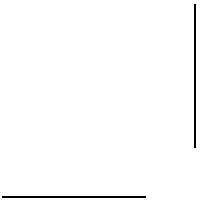
### 3.6.4 Socket and Copy register

The host uses this register to configure PC Cards to work in a twin-card environment. Although the ST7050P supports the use of this register, the drive does not currently support twin-card arrangements. This data is provided for information only.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Copy Number			Socket Number			

**Copy Number:** The host writes to this field to indicate that the card should behave as the  $n$ th copy of the card installed in the system. The first card has a copy number of 0. The last card has a copy number of  $max - 1$ , where  $max$  is the total number of cards installed in the system.

**Socket Number:** The host writes to this field to tell the card in which socket it is installed. The first socket has a socket number of 0.





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*Publication Number: 36232-001, Rev. A, Printed in USA*