

**CFS635A/CFS850A/CFS1275A**  
**Intelligent Disk Drive**  
**Product Manual**

**Production Release Per ECO 6520**  
**P/N 20401006-001**  
**Revision A**

**July 1995**

**CONNOR**<sup>®</sup>  
*The Storage Answer*

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- Relocate the computer with respect to the receiver.
- Move the computer into a different outlet so that the computer and receiver are on different branch circuits.

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# Overview of the Drive

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# 1

## What is the Drive?

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The Conner Filepro Series CFS635A/CFS850A/CFS1275A are enhanced IDE, low-profile hard disk drives that are designed to operate with an IBM PC/AT or equivalent host computer system in translate mode. The drives support advanced ATA PIO mode 4 and DMA Mode 2 data transfer protocols for superior I/O performance. Logical Block Addressing (LBA) is supported for compatibility with advanced system (BIOS) which support greater than 528 MB capacity IDE drives, as well as Cylinder-Head-Sector (CHS) addressing for backward compatibility.

<i>Drive Model:</i>	<i>Form Factor:</i>	<i>Capacity (formatted):</i>	<i>No. of disks/heads:</i>
CFS635A	inch high, 3.5 inch	635MB	2 disk/ 3 heads
CFS850A	inch high, 3.5 inch	850MB	2 disk/4 heads
CFS1275A	inch high, 3.5 inch	1275MB	3 disk/6 heads

For simplicity , we often refer to these drives collectively in this manual as “ the drive”.

## Features of the Drive

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The drive provides these features:

- can be installed in a wide range of host systems
- Task File emulation and ATA compatibility allows installation in a wide range of host systems.
- high-performance rotary voice coil actuator with embedded servoing eliminate the need for T-cal.
- one-of-seven run-length limited code.
- high shock resistance.
- Sealed head/disk assembly.
- automatic actuator latch against inner stop upon power-down.
- microprocessor-controlled diagnostic routines that are automatically executed at start-up.
- 64KB segmentable cache buffer.
- Read Look Ahead and selectable Write Caching.
- automatic error correction and retries, ECC on the fly.

- 512-byte block size.
  - Supports both CHS and LBA addressing.
  - Allows daisy-chaining up to two drives on the AT interface.
  - Auto-Translate (Universal Translate).
  - 4-byte ECC diagnostic check in read/write.
  - Supports ATA (AT attachment) interface standard.
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## ***What the Drive is Composed Of***

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The drive is composed of **mechanical**, **electrical**, and **firmware** elements.

### ***Mechanical Design Features***

The drive's hardware includes the components described in the following sections. Figure 1-1 shows some of these components.

#### ***Drive Assembly Housing***

The drive assembly housing, or Head-Disk Assembly (HDA) consists of a die cast aluminum base on which is mounted a die cast aluminum cover. A gasket seals the joint between the base and cover to retard the entry of moisture and environmental contaminants from the assembly.

This assembly, the Head-Disk Assembly, contains an integral 0.3 micron filter, which maintains a clean environment. Critical drive components are contained within this contaminant-free environment.

#### ***Drive Motor and Spindle***

A brushless DC direct-drive motor assembly is mounted on the drive's base. The motor rotates the drive's spindle at 3600 RPM. The motor/spindle assembly is dynamically balanced to provide minimal mechanical runout to the disks. A dynamic brake is used to provide a fast stop to the spindle motor and return the heads to the landing zone when power is removed.

#### ***Head Positioning Mechanism***

The read/write heads are supported by a mechanism coupled to a rotary voice coil actuator.

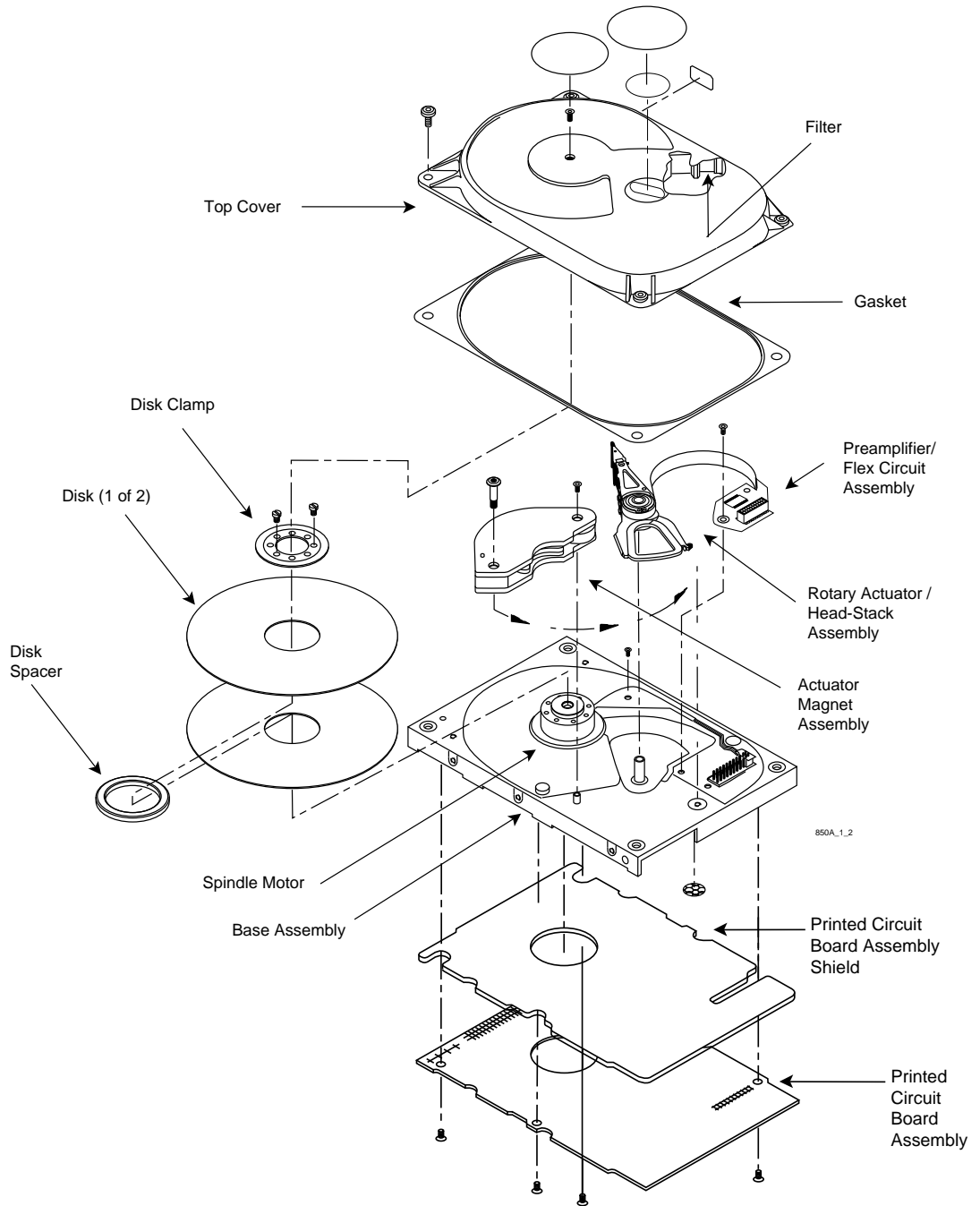
#### ***Read/Write Heads and Disks***

Data is recorded on a 95mm diameter disks through thin film or MIG heads.

The CFS635A contains two disks with three data surfaces and three read/write heads. The CFS850A contains two disks with four data surfaces and four read/write heads. The CFS1275A contains three disks with six data surfaces and six read/write heads.

At power-down, the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is separate from the data tracks.

**Figure 1-1**  
**Hard Drive Components (CFS850A)**



## **Electrical Design Features**

### **Data and Power Connections**

The drive has a single 40-pin data connector, as well as an auxiliary connector which is reserved for factory or engineering evaluation use.

Electrical power is supplied to the drive using an industry standard 4-pin power connector.

The drive also has a jumper block which can be set to specify drive operational parameters. For more information on the drive's connectors and on setting jumpers, refer to chapters 3 and 4.

### **Preamplifier**

A single integrated circuit (IC) is mounted within the head disk assembly, in close proximity to the read/write heads. The IC provides head selection, read pre-amplification, and write drive circuitry.

### **Circuit Board**

The drive's microprocessor-controlled circuit board provides the remaining electronic functions, which include:

- read/write circuitry
- rotary actuator control
- interface control
- spin speed control
- auto-park
- power management

## **Firmware**

The drive's firmware includes a command set which the host uses to control the drive. The command set allows the host to request the following types of actions:

- report drive status
- seek a specific point on the disk
- read and write data

For more information on the drive's command set, refer to chapters 6 and 7.



## ***Specifications In This Chapter***

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This chapter defines the following specifications for the drive:

- drive capacity
- physical configuration
- performance characteristics
- read/write characteristics
- reliability
- power requirements
- environmental tolerances
- safety standards
- physical characteristics

## Drive Capacity

### Formatted Capacity:

- CFS635A: 635MB
- CFS850A: 850MB
- CFS1275A: 1275MB

\* 1MB = 1 x 10<sup>6</sup> bytes

## Physical Configuration

<i>Specification</i>	<i>CFS635A</i>	<i>CFS850A</i>	<i>CFS1275A</i>
<b>Disk Type</b>	Sputtered Thin Film	Sputtered Thin Film	Sputtered Thin Film
<b>Head Type</b>	MIG/Thin Film	MIG/Thin Film	MIG/Thin Film
<b>Actuator Type</b>	Rotary Voice Coil	Rotary Voice Coil	Rotary Voice Coil
<b>Number of Disks</b>	2	2	3
<b>Data Surfaces</b>	3	4	6
<b>Data Heads</b>	3	4	6
<b>Servo</b>	Embedded	Embedded	Embedded
<b>Tracks per Surface</b>	3640	3640	3640
<b>Buffer Size</b>	64KB	64KB	64KB
<b>Track Density</b>	3849 tpi	3849 tpi	3849 tpi
<b>Formatted Track Capacity</b>	39,424 -73,216 bytes	39,424 -73,216 bytes	39,424 -73,216 bytes
<b>Bytes per Block</b>	512	512	512
<b>Blocks per Drive</b>	1,248,438	1,664,584	2,496,876
<b>Sectors per Track (User)</b>	77-143	77-143	77-143
<b>Translate</b>	Universal	Universal	Universal

\* Refer to chapter 3 for a definition of Universal Translate Mode

## Performance Characteristics

### Seek Times (typical)\* :

- Track to track: 3 ms
- Average: 14 ms \*\*
- Maximum: 26 ms

- The timing is measured through the interface with the drive operating at nominal DC input voltage and nominal operating temperature. The timing also assumes that:
  - BIOS and PC system hardware dependency have been subtracted from timing measurements
  - the drive is operated using its native drive parameters
  - the controller overhead is the time it takes to assert +HOST IRQ after the host writes the command register with a READ instruction, for the case where the data already resides in the buffer

\*\* The average seek time is determined by averaging the seek time for a minimum of 1000 seeks of random length over the surface of the disk.

### Average Latency:

- 8.33 ms

### Rotation Speed:

- 3600 RPM ( $\pm 0.1\%$ )

### Controller Overhead:

- <1.0ms

### Start Time at Power-Up: \*

- 0 RPM to 3600 RPM
  - Typical: 8.5 seconds
  - Maximum: 20 seconds
- 0 RPM to Ready
  - Typical: 15 seconds
  - Maximum: 20 seconds

\* These numbers assume spin recovery is not invoked. If spin recovery is invoked, the maximum could be 40 seconds. Briefly removing power can lead to spin recovery being invoked.

### Stop Time at Power-Down:

- Typical: 8.5 seconds
- Maximum: 20 seconds

### Interleave:

- 1:1

## **Read/Write Characteristics**

**Interface:**

- Task File

**Recording Method:**

- 1 of 7 RLL code

**Recording Density (ID):**

- 77,477 bits per inch

**Flux Density (ID):**

- 58,107 flux reversals per inch

**Data Transfer Rate:**

- To/From Media: 3.04 - 5.68 MB/second
- To/From Host: up to 16.6 MB/second

## **Reliability**

**Data Reliability:**

- < 1 non-recoverable error in  $10^{14}$  bits read

**Component Design Life:**

- 5 years

**Start/Stop Cycles:**

- 40,000 minimum

**Mean Time Between Failures:**

- 300,000 power-on hours

**Preventive Maintenance:**

- none

## Power Requirements

<i>Mode: *</i>	<b>+5 Volts (typical):</b>	<b>+12 Volts (typical):</b>	<b>Watts (typical):</b>	<b>(maximum):</b>
<b>Read/Write</b>	400mA	150mA	3.8W	4.0W
<b>Seek (100%)</b>	200mA	240mA	3.9W	5.5W
<b>Seek (30%)</b>	240mA	150mA	3.0W	3.5W
<b>Idle</b>	210mA	125mA	2.5W	3.5W
<b>Standby</b>	190mA	0mA	1.0W	1.0W
<b>Sleep</b>	175mA	0mA	0.9W	<1.0W
<b>Spin-Up</b>	300mA	1100mA	N/A	N/A

\* Refer to chapter 3 for the definitions of the modes. Spin-Up Mode current draw is for 7 seconds, maximum. Maximum power is when the supply voltage is at the worst case condition.

### Minimum/Maximum Voltage:

- +5V:  $\pm 5\%$
- +12V:  $\pm 5\%$

### Maximum Peak-to-Peak Noise Allowed (DC to 1 MHz, with equivalent resistive load):

- +5V: 2%
- +12V: 1%

## Environmental Tolerances

### Temperature:

- Operating: 5° to 55° C
- Non-operating: -40° to 60° C
- Thermal Gradient: 20° C per hour maximum

### Relative Humidity (non-condensing):

- Operating: 8 to 80%
- Non-operating: 8 to 80%
- Wet Bulb: 28.9° C maximum

### Altitude (relative to sea level):

- Operating: -200 to 10,000 feet
- Non-operating: -200 to 40,000 feet (maximum)
- Altitude Gradient: 1,000 feet/minute

### Shock (half-sine pulse, 11 ms duration):

- Operating: 5G without non-recoverable errors
- Non-operating: 75G without non-recoverable errors

**Vibration (swept-sine, one octave per minute):**

- Operating
  - 5 - 10 Hz: 0.10 inch displacement double amplitude
  - 10 - 400 Hz: 0.5G peak without non-recoverable errors
- Non-operating (swept-sine, 1/2 octave per minute):
  - 5 - 32 Hz: 0.10 inch displacement; double amplitude
  - 32 - 400 Hz: 5G peak without non-recoverable errors

**Magnetic Field:**

- The disk drive will meet its specified performance while operating in the presence of an externally-produced magnetic field under the following conditions:

Field Frequency	Intensity
DC	6 gauss
to 700 Khz	7 milligauss
700 Khz to 1.5 Mhz	3 milligauss

**Acoustic Noise:**

- The sound pressure level will not exceed 38 dBA in Idle Mode at a distance of 1 meter from the drive. The sound power level measured based on ISO 7779 will not exceed 4.3 Bel in Idle Mode.

**Safety Standards**

The drive is designed to comply with relevant product safety standards, including:

- UL 478, 5th edition, Standard for Safety of Information Processing and Business Equipment
- UL 1950, Standard for Safety of Information Technology Equipment
- CSA 22.2 #220, Information Processing and Business Equipment
- CSA 22.2 #950, Safety of Information Technology Equipment
- IEC 380, Safety of Electrically Energized Office Machines
- IEC 950, Safety of information Technology Equipment Including Electrical Business Equipment
- VDE 0805, VDE 0805 TIEL 100, and VDE 0806
- Complies with FCC Class B, Part 15, Subpart J

## Physical Characteristics

**Height:**

- 1.0 inch  $\pm$  .030

**Width:**

- 4.0 inches  $\pm$  .020

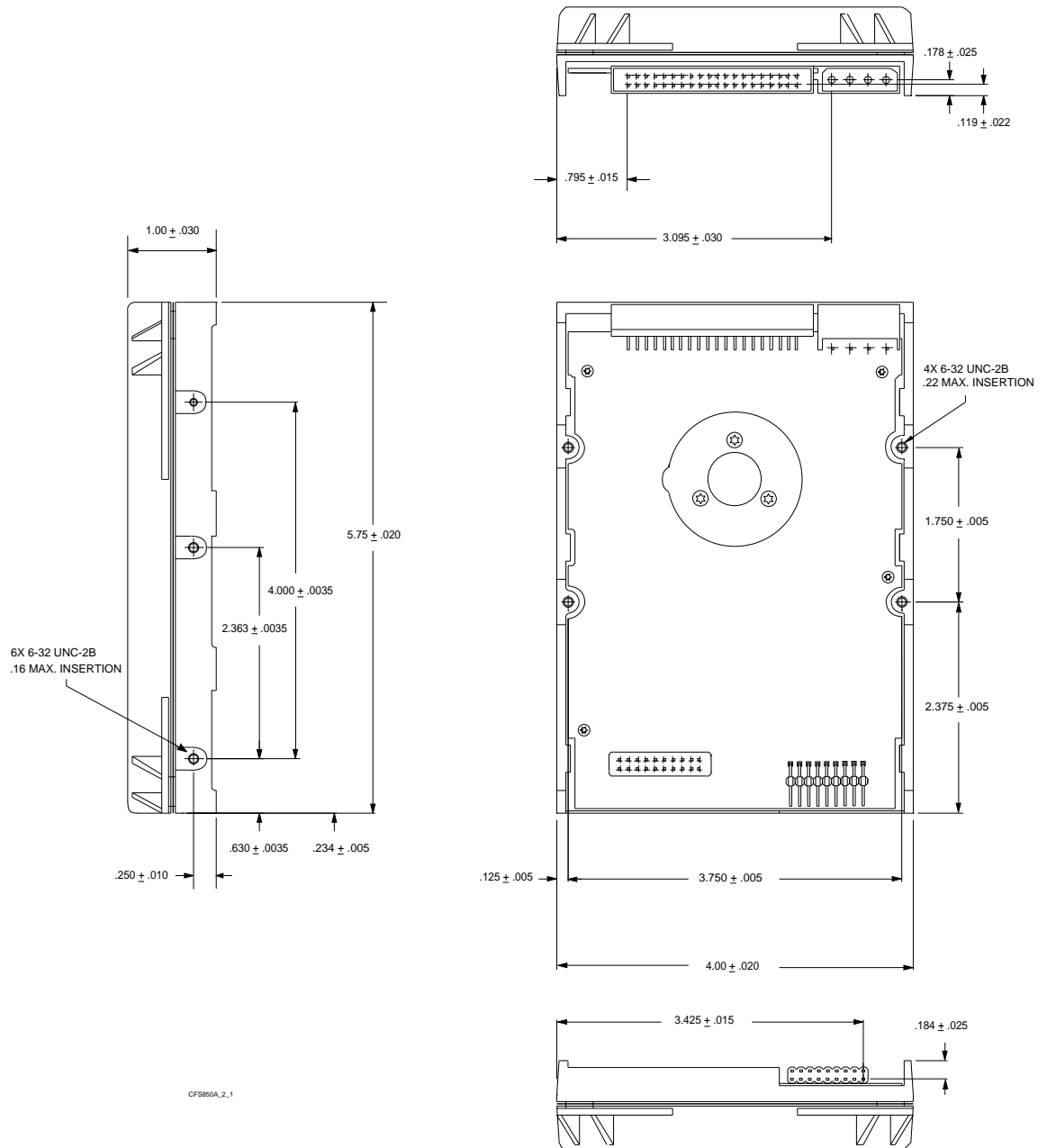
**Depth:**

- 5.75 inches  $\pm$  .020

**Weight:**

- 1.25 pounds (CFS635/CFS850A).
- 1.3 pounds (CFS1275A)

**Figure 2-1**  
**The Drive's Physical Dimensions**





## *Functions of the Drive*

---

This chapter describes certain operational aspects of the drive, including discussions of:

- drive operational modes
- error correction
- Universal Translate Mode
- master/slave configurations

## *Drive Operational Modes*

---

The drive operates in the following modes:

- **Read/Write Mode** occurs when data is read from or written to the disk.
- **Seek Mode (100%)** occurs when the actuator is in motion.
- **Seek Mode (30%)** occurs when the drive is operated in a random seek/read/write mode with a 30% seek duty cycle.
- **Idle Mode** occurs when the drive is not reading, writing, or seeking. The motor is up to speed and the **Drive Ready** condition exists. The actuator is residing on the last-accessed track.
- **Standby Mode** occurs when the motor is stopped and the actuator is parked. Standby Mode occurs after a programmable time-out since the last host access occurs. The drive will leave Standby Mode upon receipt of a command which requires disk access, or upon receipt of a spin-up command.
- **Sleep Mode** occurs when all electronics are disabled. The host is required to issue a **Reset** command to exit the Sleep Mode.
- **Spin-Up Mode** occurs while the drive is spun up to speed after being powered on or after exiting Standby or Sleep Mode.

## *Error Correction*

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The drive uses a Reed-Solomon code to perform error detection and correction. For each 512-byte block, the software error correction polynomial is capable of correcting:

- one error burst up to 22 bits
- two error bursts up to 11 bits each

Single bursts of 11 bits or less are corrected on the fly (OTF) with no performance degradation.

## Universal Translate Mode

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Conner has established a Universal Translate Mode which enables you to configure the drive in an AT environment to any cylinder, head, and sector configuration desired. The translate configuration is limited by the maximum capacity of the drive and host system parameters. Upon initial power-up of the drive, it will default to the configuration shown below:

<i>Drive:</i>	<i>No. of Cylinders:</i>	<i>No. of Heads</i>	<i>No. of Sectors:</i>
CFS635A	1238	16	63
CFS850A	1651	16	63
CFS1275A	2477	16	63

After the drive is ready, the host system may issue an **Init Drive Parm**s command (command code 91 hex) to alter the translate configuration (number of heads and number of sectors per track). The drive will then:

- calculate the total number of available logical tracks based upon the entered sector and head values
- save the drive parameters in non-volatile memory for subsequent drive operations

## Master/Slave Configuration


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When two drives are daisy-chained on the host interface, one must be designated as the **master drive** (C: drive) and one as the **slave drive** (D: drive). Commands from the host are written in parallel to both drives.

When the C/D jumper on the drive is closed, the drive will assume the role of a master. When C/D is open, the drive will act as a slave. In single-drive configurations, C/D must remain in the closed (master) position. For more information on setting the C/D jumper, refer to chapter 4.

For each command sent from the host, the DRV bit in the Device/Head register selects the master or the slave drive. When the DRV bit is reset (0), the master drive is selected, and when the DRV bit is set (1), the slave drive is selected.

Once the drives receive the command, only the drive with jumper C/D set to the appropriate position will execute the command. For example, if the DRV bit is set, only the slave drive (jumper C/D open) will execute the command.

 **Note:** If the command is a diagnostic command, both drives will execute the command and the slave will report its status to the master via the Host PDIAG signal.

**Drive selection** always refers to the state of the DRV bit in the Device/Head register and the position of the C/D jumper throughout this manual.

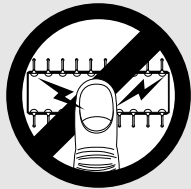
**Cable Select**

This optional method of drive master/slave designation can be enabled by jumper selection as described in Chapter 4. If used, special cabling can be used to selectively ground the CSEL interface signal of the drive intended to be drive C (0). This drive will then function as the master. If CSEL is allowed to float the drive will recognize itself as drive D (1) and function as the slave.



### ***Take These Precautions***

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To protect your equipment from electrostatic damage, perform the installation at a static-safe workstation. If one is not available, follow these guidelines:

1. Work in an uncarpeted area.
2. Before removing the equipment from its anti-static bag, discharge static electricity by touching your computer's metal chassis (or any other grounded object) while touching the anti-static bag.
3. Do not touch circuit boards unless instructed to do so.

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### ***Installing the Drive***

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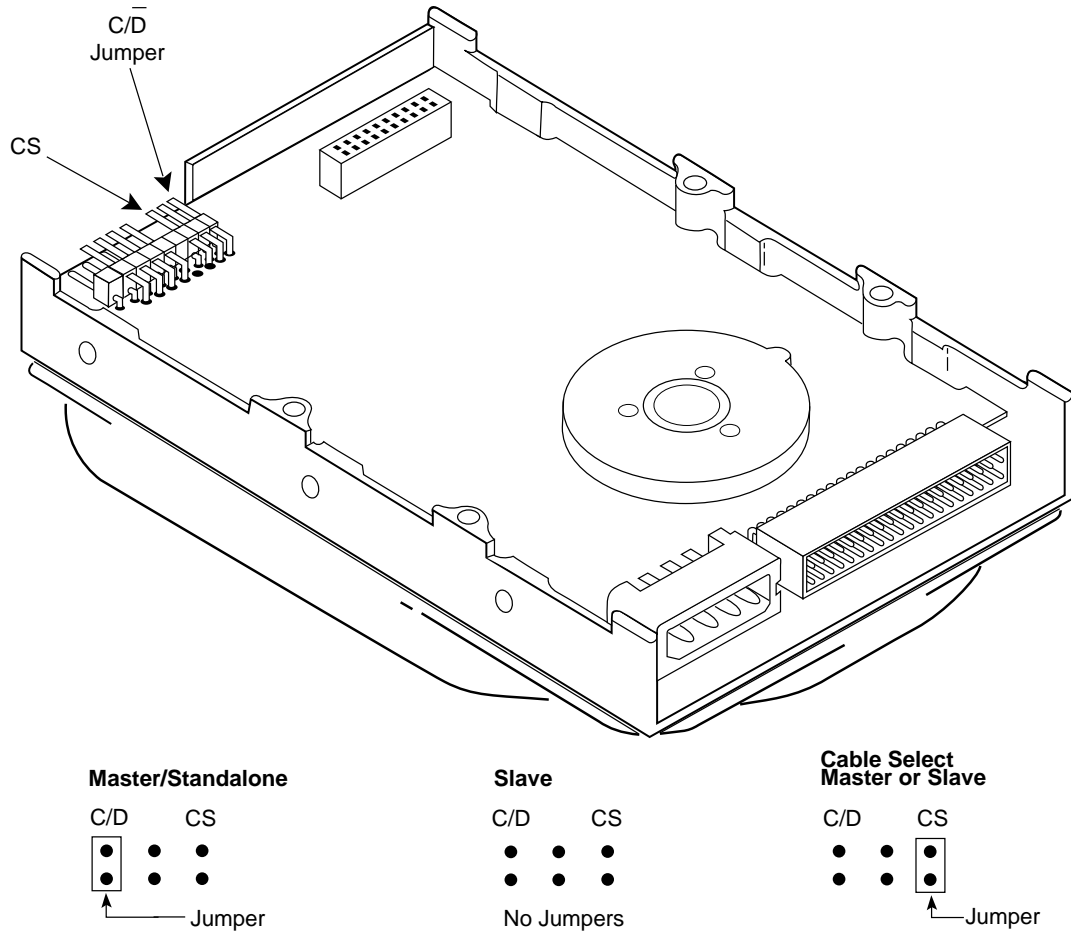
To install the drive, you must:

- set the drive's jumpers, if desired
- attach a data cable to the drive
- attach power to the drive
- mount the drive

**Setting the Drive's Jumpers**

Figure 4-1 shows you how to access the drive's jumpers.

**Figure 4-1  
Jumper Locations**



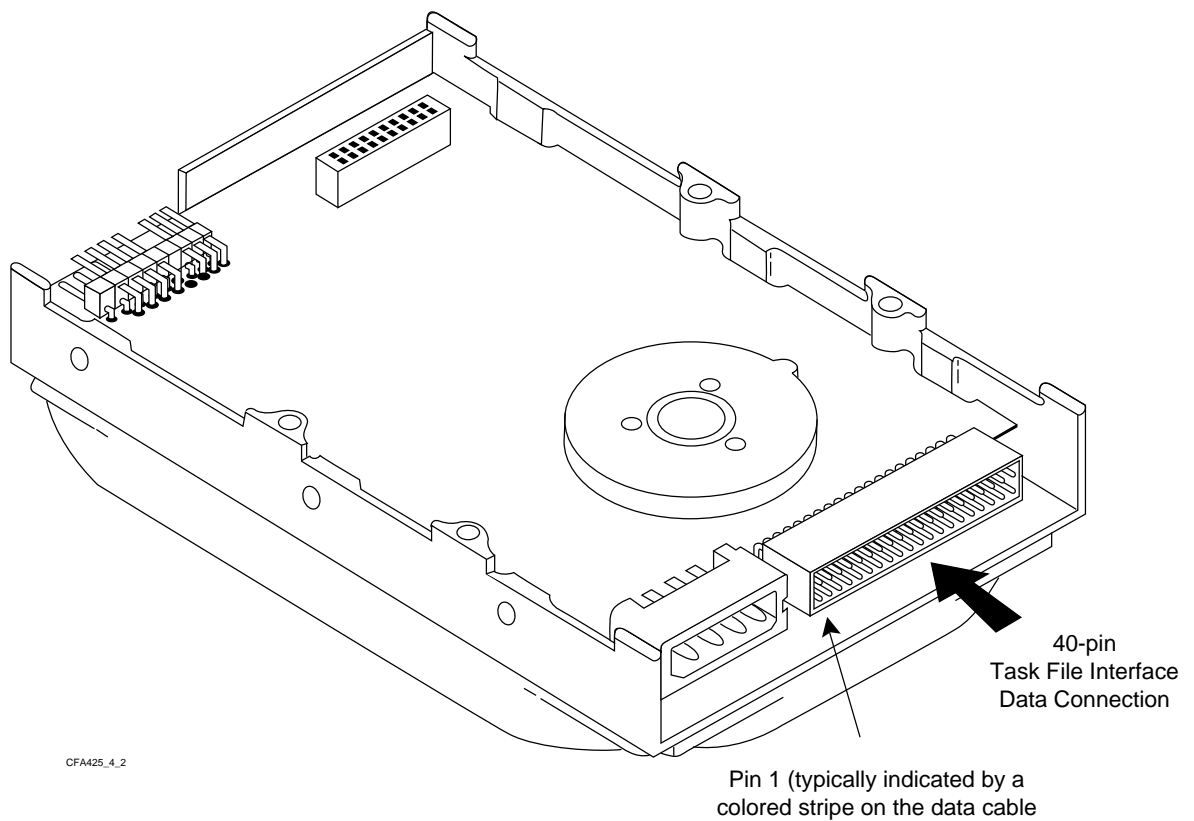
Here is how you can set these jumpers. Pins described as “reserved” should not be used.

<b>Pins:</b>	<b>Signal:</b>	<b>Description</b>
<b>1 and 2</b>	C/D	Open: Drive will act as slave. Closed: Drive will act as master.
<b>3 and 4</b>	N/C	Reserved
<b>5 and 6</b>	CS	Open: Cable select option disabled closed: Cable Select enabled
<b>Note:</b>		<i>When using C/S option, the C/D jumper must be open</i>
<b>7 to 18</b>	N/A	Reserved

## Attaching a Data Cable to the Drive

Attach the data cable from the host to the Task File Interface connector, as shown in figure 4-2. Refer to the table on the following page for pinout information.

**Figure 4-2**  
**Attaching a Data Cable**



**Caution:** Do not route the data cable next to the drive PCB or any other high frequency or large current switching signals. Improper drive operation can result from improper cable routing.

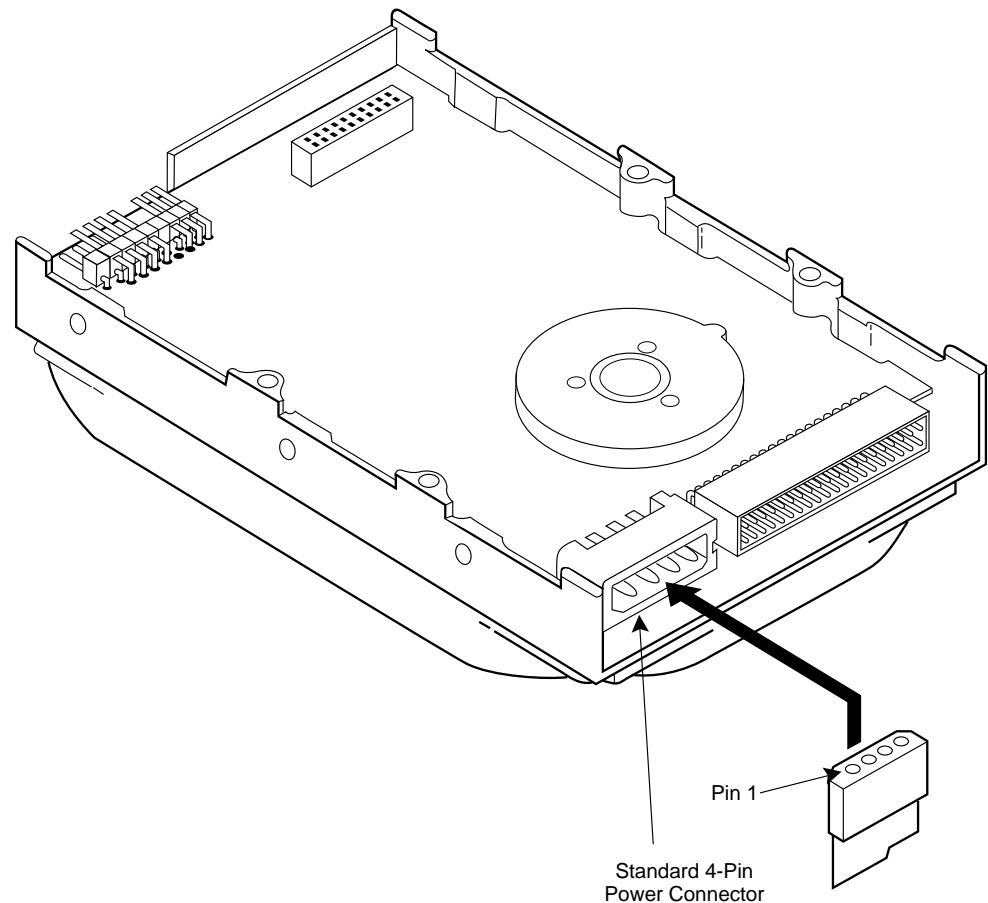
<b>Pin:</b>	<b>Signal:</b>	<b>Pin:</b>	<b>Signal:</b>
01	- HOST RESET	02	GND
03	+ HOST DATA 7	04	+ HOST DATA 8
05	+ HOST DATA 6	06	+ HOST DATA 9
07	+ HOST DATA 5	08	+ HOST DATA 10
09	+ HOST DATA 4	10	+ HOST DATA 11
11	+ HOST DATA 3	12	+ HOST DATA 12
13	+ HOST DATA 2	14	+ HOST DATA 13
15	+ HOST DATA 1	16	+ HOST DATA 14
17	+ HOST DATA 0	18	+ HOST DATA 15
19	GND	20	KEY
21	+ DMARQ	22	GND
23	- HOST IOW	24	GND
25	- HOST IOR	26	GND
27	+ IOCHRDY	28	+ CSEL (optional)
29	- DMACK	30	GND
31	+ HOST IRQ14	32	- HOST IO16
33	+ ADDR1	34	- HOST PDIAG
35	+ ADDR0	36	+ ADDR2
37	- HOST CS0	38	- HOST CS1
39	- DASP	40	GND

The recommended mating connector for the Task File Interface is Molex P/N 15-47-5401 or equivalent. You may daisy-chain two drives on this connector. The maximum cable length is 18 inches.

## Attaching Power to the Drive

The drive has a standard 4-pin DC power connector.

**Figure 4-3**  
**Attaching a Power Cable**



**Caution:** Do not route the power cable next to the drive PCB or any other high frequency or large current switching signals. Improper drive operation can result from improper cable routing.

The following table describes the 4-pin power connector pins:

<b>Pin:</b>	<b>Signal:</b>
1	+12 Volts
2	GND
3	GND
4	+5 Volts

The mating connector for the 4 pin connector is AMP 1-480424-0 (housing) and AMP 60619-4 (loose piece) or 61117-4 (strip) contacts.

## Mounting the Drive

You can mount the drive either vertically or horizontally. The drive will meet all performance specifications when mounted at any orientation.



**Caution:** The surface(s) on which you mount the drive should be flat and parallel to prevent uneven pressure on the drive. Mounting the drive on an uneven surface could cause the drive's base to deform, degrading drive performance.



**Caution:** When using the side mounting holes, verify the screw length to ensure clearance from the drive's printed circuit board before tightening the screw.

Refer to figure 2-1 in chapter 2 for dimensions and the location of mounting screw holes.

## About the Host Interface

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The interface between the drive adapter and the drive is called the **host interface**. The set of registers in the I/O space of the host that are controlled through the host interface is known as the **task file**.

The physical interface from the drive to the host is called the **task file interface** and is implemented using a 40-pin connector. The pin assignments were described in chapter 4.

Definitions of signals are listed beginning on the next page under **Signal Descriptions**.

## Signal Conventions

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The following conventions are used in the discussions that follow:

- All signals on the host interface shall have the prefix HOST.
- All negatively-active signals shall be further prefixed with a “-” designation.
- All positive-active signals shall be prefixed with a “+” designation.
- Signals whose source is the host are said to be “outbound” and those whose source is the drive are said to be “inbound.”

## Signal Levels

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All signal levels are TTL compatible. A logic “1” is >2.0 Volts. A logic “0” is from 0.00 Volts to 0.70 Volts. The drive capability of each of the inbound signals is described below.

## Signal Descriptions

The following table describes signals on the task file interface.

<b>Signal Name:</b>	<b>Dir:</b>	<b>Pin:</b>	<b>Description:</b>
-HOST RESET	O	1	Reset signal from the host system which is active low during power-up and inactive thereafter.
GND	O	2, 19, 22, 24, 26,30, 40	Ground between the drive and the host.
+HOST DATA	I/O	3 - 18	16-bit bi-directional data bus 0 - 15 between the host and the drive. The lower 8 bits, HD0 - HD7, are used for register and ECC access. All 16 bits are used for data transfers. These are tri-state lines with 24 mA drive capability.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
+DMARQ	I	21	Host DMA request handshake signal.
-HOST IOW	O	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 - HD15, into a task file register or the data register on the drive.
-HOST IOR	O	25	Read strobe, which when low enables data from the Task File on the drive onto the host data bus, HD0 - HD15. The rising edge of -HOST IOR latches data from the drive at the host.
+IOCHRDY	I	27	This signal is negated to extend host transfer cycles when the controller is not ready to respond.
+CSEL	I/O	28	Cable Select is functional when the C/S jumper is inserted, which routes the C/D select to this pin. When set high, drive D: is selected; when set low, drive C: is selected.
-DMACK	O	29	Host DMA acknowledge handshake signal.
+HOST IRQ14	I	31	Interrupt to the host system, enabled only when the drive is selected and the host activates the -IEN bit in the Device Control register. When the -IEN bit is inactive or when the drive is not selected, this output is in a high impedance state, regardless of the state of the IRQ bit.
			IRQ is reset to zero by a host read of the Status register after completion of a data transfer phase or a write to the Command register. This signal is a tri-state line with 8 mA drive capacity.

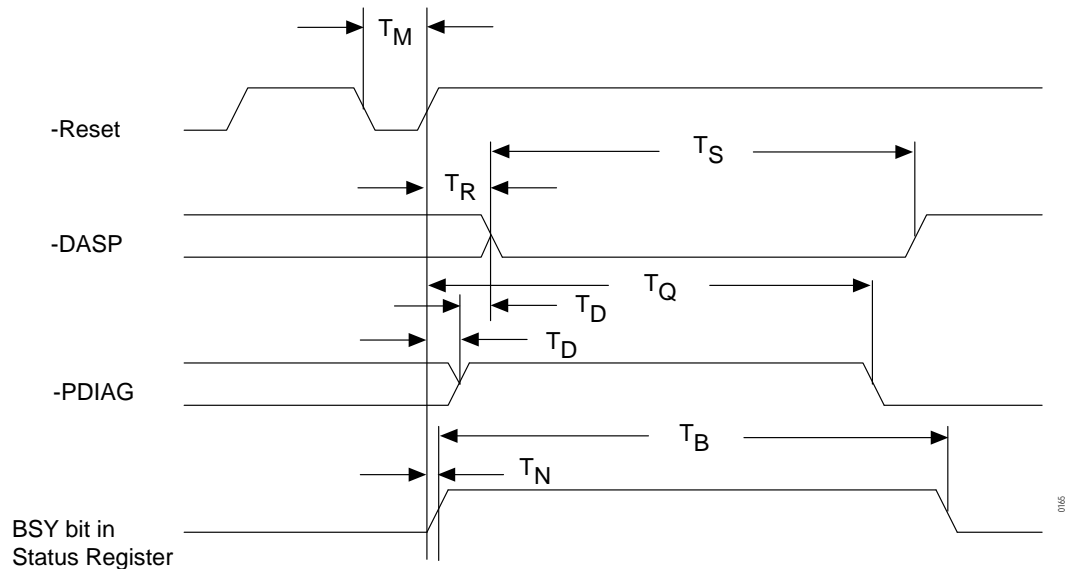
<b>Signal Name:</b>	<b>Dir:</b>	<b>Pin:</b>	<b>Description:</b>
-HOST IO16	I	32	Indication to the host system that the 16-bit data register has been addressed and that the drive is prepared to send or receive a 16-bit data word. This line is tri-state line with 24 mA drive capacity.
-HOST PDIAG	I	34	<p>This signal shall be asserted by the slave to the master that it has completed diagnostics. A 10K ohm pull-up resistor shall be used on this signal by each drive.</p> <p>Following a POR, a software reset, or a RESET-, the slave will negate PDIAG- within 1 ms (to indicate to the master that it is busy). The slave will then assert PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status. After the assertion of PDIAG-, the slave may be unable to accept commands until it has finished its reset procedure and is ready (DRDY =1).</p> <p>Following the receipt of a valid Execute Drive Diagnostics command, the slave will negate PDIAG- within 1 ms to indicate to the master that it is busy and has not yet passed its drive diagnostics. If the slave is present, then the master will wait for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for the slave to assert PDIAG-. The slave should clear BSY before asserting PDIAG-, as PDIAG- is used to indicate that the slave has passed its diagnostics and is ready to post status.</p> <p>If DASP- was not asserted by the slave during reset initialization, the master will post its own status immediately after it completed diagnostics and clear the slave status register to 00 hex. The master may be unable to accept commands until it has finished its reset procedure and is Ready (DRDY = 1).</p>
+HOST A0,A1,A2	O	35, 33, 36	Bit binary coded address used to select the individual registers in the task file.
-HOST CS0	O	37	Chip select decoded from the host address bus. Used to select most of the host-accessible registers.
-HOST CS1	O	38	Chip select decoded from the host address bus. Used to select three of the registers in the task file.

<b>Signal Name:</b>	<b>Dir:</b>	<b>Pin:</b>	<b>Description:</b>
-DASP	I	39	<p>DASP- (drive active/slave present). This is a time-multiplexed signal which indicates that a drive is active, or that the slave is present. This signal is an open-collector output and each drive has a 10K pull-up resistor.</p> <p>During power-on initialization or after RESET is negated, DASP- shall be asserted by the slave within 400 ms to indicate that the slave is present.</p> <p>The master shall allow up to 450 ms for the slave to assert DASP-. If the slave is not present, the master may assert DASP- to drive an activity LED.</p> <p>DASP- shall be negated following acceptance of the first valid command by drive 1 or after 31 seconds, whichever comes first.</p> <p>Any time after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.</p>

### ATA/CAM Master/Slave Reset Timing

Figure 5-1 illustrates the ATA/CAM Master/Slave reset sequence.

**Figure 5-1**  
**ATA/CAM Reset Sequence**



<i>Description</i>	<i>Label</i>	<i>POR Value</i>	<i>Soft Reset Value</i>
-Reset width (min)	$T_M$	25 $\mu$ s	N/A
-DASP asserted (max)	$T_S$	31s	31s
-DASP after Reset (max)	$T_R$	450ms	N/A
Slave DIAG complete (max)	$T_Q$	30s	30s
Drive BSY (max)	$T_B$	31s	31s
-DASP after -PDIAG (min)	$T_D$	>0	N/A
BSY status after Reset (max)	$T_N$	400ns	400ns
-PDIAG after Reset (max)	$T_A$	N/A	1ms

**Notes:**

1. -DASP is asserted by both the master and the slave. The signal on the bus is the “wired OR” of -DASP from both drives. The master de-asserts -DASP within 1ms after reset and waits for up to 450ms for the slave to assert -DASP to signal its presence.
2. During a reset condition, the host BIOS checks drive 0 for BSY to be reset. Drive 0 monitors the -PDIAG signal from the slave. When the slave completes its diagnostics, it clears its BSY and asserts -PDIAG. The master will wait for up to 31 seconds for -PDIAG, then clears its BSY and de-asserts -DASP.

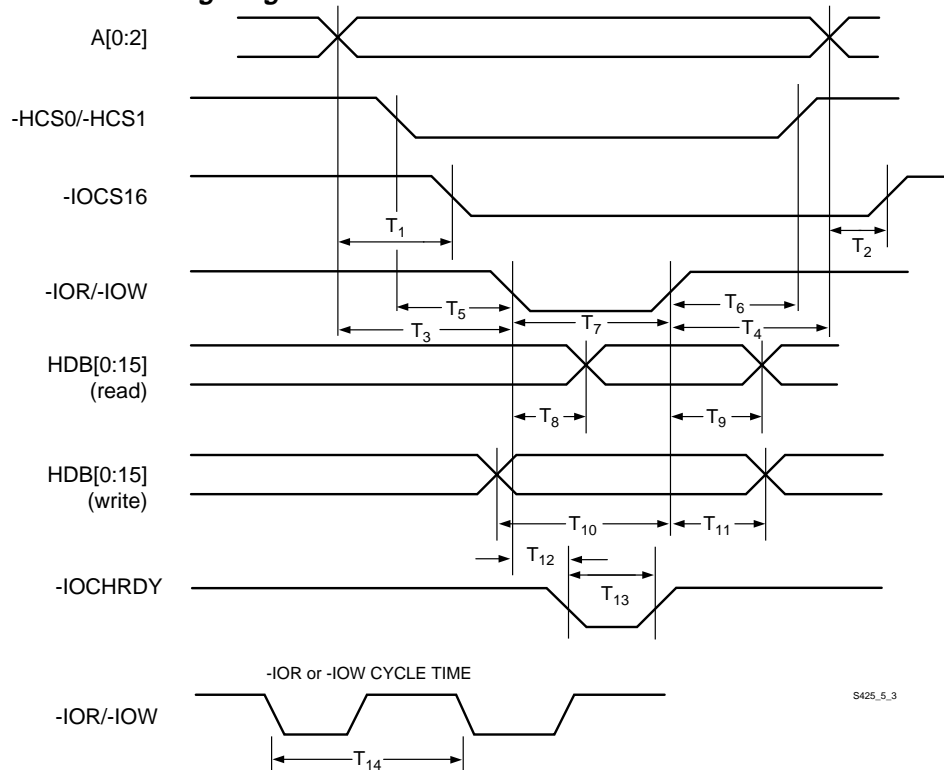
## Host PIO 16-Bit Timing Values

The values\* in the table below refer to the timing diagram in figure 5-3.

Symbol	Parameter Units	Min:	Max:	Unit:
T <sub>1</sub>	A[0:2] valid until -IOCS16 valid		20	ns
T <sub>3</sub>	A[0:2] valid until -IOR or -IOW valid	20		ns
T <sub>4</sub>	A[0:2] valid after -IOR or -IOW invalid	5		ns
T <sub>5</sub>	-CS0 or -CS1 valid until -IOR or -IOW valid	20		ns
T <sub>6</sub>	-CS0 or -CS1 valid after -IOR or IOW invalid	5		ns
T <sub>7</sub>	-IOW or -IOR pulse width	50		ns
T <sub>8</sub>	Read Data valid after -IOR valid		30	ns
T <sub>9</sub>	Read Data valid after -IOR invalid	5		ns
T <sub>10</sub>	Write Data valid until -IOW invalid	20		ns
T <sub>11</sub>	Write Data valid after -IOW invalid	5		ns
T <sub>12</sub>	-IOR or -IOW valid until -IOCHRDY valid		20	ns
T <sub>13</sub>	-IOCHRDY pulse width		1,250	ns
T <sub>14</sub>	-IOR/-IOW cycle time (w/ IOCHRDY)	120		ns

\* Under conditions equivalent to a 330 ohm pullup and a 56pf load. Cable type and length may affect the values measured at the drive or host interface.

**Figure 5-3**  
**Interface PIO Timing Diagram**



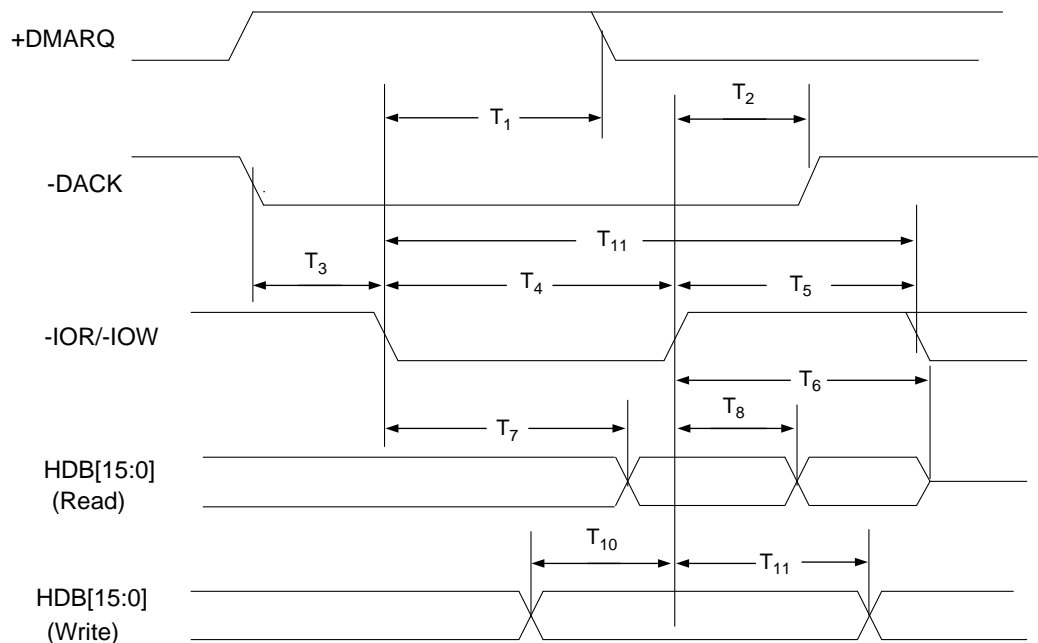
## Host Demand Mode DMA 16-bit Interface Timing Values

The values\* in the table below refer to the timing diagram in figure 5-4.

Symbol	Parameter:	Min:	Max:	Units:
T <sub>1</sub>	+DMARQ low from -IOR/-IOW low		35	ns
T <sub>2</sub>	-DACK hold from -IOR/-IOW high	5		ns
T <sub>3</sub>	-DACK low to -IOR/-IOW low	0		ns
T <sub>4</sub>	-IOR/-IOW pulse width	50		ns
T <sub>5</sub>	-IOR/-IOW high	30		ns
T <sub>6</sub>	-IOR low to HDB[15:0] valid		30	ns
T <sub>7</sub>	-IOR high to HDB[15:0] invalid	5		ns
T <sub>8</sub>	-IOR high to HDB[15:0] tri-state		30	ns
T <sub>9</sub>	HDB[15:0] set-up to -IOW high	20		ns
T <sub>10</sub>	HDB[15:0] hold from -IOW high	5		ns
T <sub>11</sub>	-IOR/-IOW cycle time	120		ns

\* Under conditions equivalent to a 330 ohm pull-up and a 56pf load. Cable type and length may affect the values measured at the drive or host interface

**Figure 5-4**  
Interface DMA Timing Diagram



S425\_5\_4



## ***Host Address Decoding***

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The host computer addresses the drive using programmed I/O. This method requires that:

- a proper **chip select** be asserted
- the desired **register address** be placed on the three host address lines (HA2 - HA0)
- a **Read** or **Write** strobe (-HOST IOR/-HOST IOW) is given to the chip

The host generates two independent chip selects on the interface.

- The high order chip select, -HOST CS1, is used to access register 3F6 or 3F7.
- The low order chip select, -HOST CS0, is used to address registers 1F0 through 1F7.

ECC bytes are transferred on bits 7 - 0.

The host data bus 15 - 8 is only enabled when:

- -IO16 is active
- the host is addressing the data register for transferring data
- the host is not transferring ECC bytes, which are only transferred if the operation is a **Read Long** or **Write Long**

The I/O map on the next page defines all of the register addresses and the functions for these I/O locations.

The sections that follow the I/O map describe each of the registers.

<b>Addr*</b>	<b>-CS0</b>	<b>-CS1</b>	<b>HA2</b>	<b>HA1</b>	<b>HA0</b>	<b>Read Function</b>	<b>Write Function</b>
	1	1	x	x	x	No Operation	No Operation
	0	0	x	x	x	Invalid Address	Invalid Address
	1	0	0	x	x	High Impedance	Not Used
	1	0	1	0	x	High Impedance	Not Used
<b>1F0</b>	0	1	0	0	0	Data Register	Data Register
<b>1F1</b>	0	1	0	0	1	Error Register	Features Register
<b>1F2</b>	0	1	0	1	0	Sector Count	Sector Count
<b>1F3</b>	0	1	0	1	1	Sector Number	Sector Number
<b>1F4</b>	0	1	1	0	0	Cylinder Low	Cylinder Low
<b>1F5</b>	0	1	1	0	1	Cylinder High	Cylinder High
<b>1F6</b>	0	1	1	1	0	Device/Head Register	Device/Head Register
<b>1F7</b>	0	1	1	1	1	Status Register	Command Register
<b>3F6</b>	1	0	1	1	0	Alternate Status Register	Device Control Register
<b>3F7</b>	1	0	1	1	1	Device Address Register	Not Used

x = don't care

\* These I/O port addresses are listed for programmer reference. They are a function of I/O decoding in the Host Adapter. These addresses are required for compatibility with most AT BIOS.

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## Addressing the Data

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There are two methods of addressing the sectors on the disk drive.

### **Cylinder-head-sector (CHS) mode**

The first method, which is the traditional approach, uses Cylinder-Head-Sector (CHS) addressing. Most disk drives today exceed the number of cylinders limit of DOS or use zone recording (different number of sectors per track in each zone) so the parameters reported by the drive in the **Identify Device** command are logical translations done by the drive. Logical translation within the drive limits DOS to 528 MB because of the combined limitations of DOS and the traditional definition of the IDE registers. BIOS and Device Drivers may provide another layer of translation to map the DOS accessible address space to the IDE register accessible address space.

Some non-DOS operating systems utilize additional bits in the Cylinder High register to go beyond the DOS limit.

### **Logical Block Addressing (LBA) Mode**

The second method uses Logical Block Addressing (LBA), which is common to SCSI. This method re-defines the content of the Task File registers, which are described later in this chapter. This drive operates with either CHS or LBA addressing by responding to the switch in the **Device/Head** register. The registers affected by LBA mode are the **Sector Number, Cylinder Low, Cylinder High, and Device/Head**. The use of these registers allows a 28-bit address space capable of handling up to 128GB of data.

In LBA mode, the sectors on the disk are linearly mapped with the first logical block (LBA 0) defined as cylinder 0, Head 0, Sector 1. The subsequent logical blocks are defined by the formula:

$$\text{LBA} = [(\text{cylinder} * \text{no. of heads} + \text{heads}) * \text{sectors/track}] + (\text{sector} - 1)$$

## ***Descriptions of the Registers***

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The following sections describe the registers used for read and write functions. In these descriptions, unused write bits should be treated as “don’t cares” and other unused bits should be read as zeroes.

### ***Data Register***

<b>Port Select:</b>	1F0
<b>Chip Select:</b>	HOST CS0
<b>Register Address:</b>	0
<b>Function:</b>	Read/Write

**Description:** This is the register:

- through which all data is passed on **Read** and **Write** commands
- to which the sector table is transferred during **Format** commands
- to which data associated with the **Identify** command is transferred

All transfers are high speed 16-bit I/O operations except for ECC bytes transferred during **R/W Long** commands, which are slower 8-bit operations that occur after the transfer of the data.

Data is stored on the disk with the Least Significant Byte (LSB) first, then the Most Significant Byte (MSB) for each word. This is important to remember when testing the ECC circuitry.

## Error Register

**Port Address:** 1F1  
**Chip Select:** -HOST CS0  
**Register Address:** 1  
**Function:** Read only

**Description:** This register contains status from the last command executed by the drive.

The contents of this register are only valid when the error bit (ERR) is set in the Status Register, unless the drive has just powered up or completed execution of its internal diagnostic, in which case the register contains a status code. The status codes are discussed in chapter 7 in the description of the **Diagnostic** command.

The bits in the register are defined below:

<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
BBK	UNC	not used	IDNF	not used	ABRT	TK0	not used

where:

- **BBK** indicates that a bad block mark was detected in the requested sector's ID field. A bad block mark is not created in the factory, but only when requested in the format command.
- **UNC** indicates that a non-correctable data error has been encountered.
- **IDNF** indicates that the requested sector's ID field could not be found.
- **ABRT** indicates that the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.
- **TK0** indicates that track 0 has not been found during a recalibrate command.

For other drives Bit 0 is AMNF (Address Mark Not Found.) This is not used on Conner drives.

## Features Register (formerly Write Precomp Register)

<b>Port Address:</b>	1F1
<b>Chip Select:</b>	-HOST CS0
<b>Register Address:</b>	1
<b>Function:</b>	Write only

**Description:** This register was previously used to set write precompensation in non-intelligent (pre-IDE) disk drives. This drive uses this register for commands EF and F1 through F6. The ATA specification defines this register as the **Features** register.

## Sector Count

<b>Port Address:</b>	1F2
<b>Chip Select:</b>	-HOST CS0
<b>Register Address:</b>	2
<b>Function:</b>	Read/Write

**Description:** This register defines the number of sectors of data to be transferred on read or write commands.

If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read, such that the register contains the number of sectors left to access in the event of an error in a multi-sector operation.

The contents of this register define the number of sectors per track when executing an **Initialize Device Parameters** command. This register is also used in the power commands to provide the power-down time-out parameter and status.

## Sector Number

<b>Port Address:</b>	1F3
<b>Chip Select:</b>	-HOST CS0
<b>Register Address:</b>	3
<b>Function:</b>	Read/Write

**CHS Description:** This register contains the starting sector number for any disk access.

**LBA Description:** This register contains bits 0-7 of the logical block address.

At the completion of each sector and at the end of the command, this register is updated to reflect the last sector read correctly or the sector on which an error occurred. During multiple sector transfers, this register is updated to point at the next sector to be read/written if the previous sector's operation was successful.

## Cylinder Low

**Port Address:** 1F4  
**Chip Select:** -HOST CS0  
**Register Address:** 4  
**Function:** Read/Write

**CHS Description:** This register contains the low-order 8 bits of the starting cylinder number for any disk access.

**LBA Description:** This register contains bits 8-15 of the logical block address.

At the completion of each sector and at the end of the command, this register is updated to reflect the current cylinder number.

## Cylinder High

**Port Address:** 1F5  
**Chip Select:** -HOST CS0  
**Register Address:** 5  
**Function:** Read/Write

**CHS Description:** This register contains the high-order bits of the starting cylinder number for any disk access. Non-enhanced BIOS will only use the first two bits of this register, forming a 10-bit cylinder address.

**LBA Description:** This register contains bits 16-23 of the logical block address.

At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

## Device/Head Register

**Port Address:** 1F6  
**Chip Select:** -HOST CS0  
**Register Address:** 6  
**Function:** Read/Write

**Description:** This register contains the drive and head numbers, as defined below:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	LBA	1	DRV	HEAD			

where:

- **DRV** is the binary encoded drive select number. When this bit is reset, the master drive is selected, and when this bit is set, the slave drive is selected. While both drive's Task File registers are always written, this bit selects which drive will respond and execute a command.
- **LBA** is the binary coded address mode select. When L = 0, addressing is by CHS mode. When L = 1, addressing is by LBA mode. This bit was RSVD (reserved) for use by the host and set to 0 prior to introduction of LBA.
- **HEAD**

**CHS Description:** This is the four-bit binary encoded head select number.

**LBA Description:** This register contains bits 24-27 of the logical block address.

At the completion of each sector and at the end of the command, this register is updated to reflect the currently selected head.

## Status Register

**Port Address:** 1F7  
**Chip Select:** -HOST CS0  
**Register Address:** 7  
**Function:** Read only

**Description:** This register contains the drive/controller status. The contents of this register are updated at the completion of each command.

If the Busy bit is active, no other bits are valid. The host reading this register when an interrupt is pending is considered to be the interrupt acknowledge, and any pending interrupt is therefore cleared whenever this register is read.

The bits in this register are defined below:

<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

where:

- **BSY** is the Busy bit, which is set whenever the drive has access to the Task File registers and the host is locked out from accessing the Task File. This bit is set under any the following circumstances:
  - At activation of the Host Reset pin in the interface, or at activation of the software reset bit in the digital output register.
  - Immediately upon host write of the command register with a **Read**, **Read Long**, **Read Buffer**, **Seek**, **Recalibrate**, **Initialize Device Parameters**, **Read Verify**, **Identify**, or **Execute Drive Diagnostic** command.
  - Immediately following transfer of 256 words of data after host write of the command register with a **Write**, **Format Track**, or **Write Buffer** command.
  - Immediately following transfer of 256 words of data and the ECC bytes after a host write of the Command register with a **Write Long** command.

When BSY is active, any host read of a Task File register is inhibited and the Status register is read instead.

- **DRDY** is the drive ready indication. When there is an error, this bit is not changed until the Status register is read by the host, at which time the bit again indicates the current readiness of the drive. This bit will be reset at power-up and remain reset until the drive is up to speed and ready to accept a command.

- **DWF** is the drive write fault bit. When there is an error, this bit is not changed until the Status register is read by the host, at which time the bit again indicates the current write fault status.
- **DSC** is the drive seek complete bit. It is an indication that the actuator is on track. When there is an error, this bit is not changed until the Status register is read by the host, at which time the bit again indicates the current readiness of the drive. This bit will be reset at power-up and will remain reset until the drive is up to speed and ready to accept a command.
- **DRQ** is the data request bit, which indicates that the drive is ready for transfer of a word or a byte of data between the host and the Data register.
- **CORR** is the corrected data bit, which is set:
  - when a correctable data error has been encountered and the data has been corrected
  - on a read verify if any sector was corrected the bit is valid

This condition will not terminate either a **Multi-Sector Read** or a **Read Multiple** command.

- **IDX** is the index bit which is set once per disk revolution. This function is not updated by this drive.
- **ERR** is the error bit, which indicates that the previous command ended in some type of error. The other bits in the Status register, as well as the bits in the Error register, will have additional information as to the cause of the error.

## Alternate Status Register

**Port Address:** 3F6  
**Chip Select:** -HOST CS1  
**Register Address:** 6  
**Function:** Read only

**Description:** This register contains the same information as the Status register in the Task File. The only difference is that reading this register does not imply interrupt acknowledge to reset a pending interrupt.

The bits in this register are defined below:

<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

See the description of the Status register for definitions of the bits in this register.

## Device Control Register

**Port Address:** 3F6  
**Chip Select:** -HOST CS1  
**Register Address:** 6  
**Function:** Write only

**Description:** This register contains two control bits as follows:

<i>Bit 7</i>	<i>Bit 6</i>	<i>Bit 5</i>	<i>Bit 4</i>	<i>Bit 3</i>	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
not used	not used	not used	not used	not used	SRST	-IEN	not used

where:

- **SRST** is the host software reset bit. The drive is held reset when this bit is active, and enabled when this bit is inactive.
- **-IEN** is the enable bit for this disk drive interrupt to the host.
  - When this bit is active (=0) and the drive is selected, the host interrupt, +IRQ, is enabled through a tri-state buffer to the host.
  - When this bit is inactive (=1), or the drive is not selected, the +IRQ pin will be in a high impedance state, regardless of the presence or absence of a pending interrupt.

## Drive Address Register

**Port Address:** 3F7  
**Chip Select:** -HOST CS1  
**Register Address:** 7  
**Function:** Read only


**Description:** This register loops back the drive select and head select addresses of the currently selected drive.

The bits in this register are as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSVD	-WTG	-HS3	-HS2	-HS1	-HS0	-DS1	-DS0

where:

- **RSVD** is reserved and negated by the drive. When the host reads the drive address register, this bit must be in a high impedance state.
- **-WTG** is the write gate bit, which is active when writing to the disk drive is in progress.
- **-HS3 through -HS0** are the one's complement of the binary coded address of the currently-selected head. For example, if -HS3 through -HS0 are 1 1 0 0, respectively, head 3 is selected.
- **-DS1** is the drive select bit for drive 1, and should be active when drive 1 is selected and active.
- **-DS0** is the drive select bit for drive 0, and should be active when drive 0 is selected and active.

 **Note:** Bit 7 is not driven for compatibility with the floppy drive address space. If your system is different, you may have to drive this bit when this register is read.

## Command Register

**Port Address:** 1F7  
**Chip Select:** -HOST CS0  
**Register Address:** 7  
**Function:** Write only

**Description:** The eight-bit code written to this register passes the command from the host to the drive. Command execution begins immediately after this register is written.

Refer to chapter 7 for a list of executable commands with the command codes and necessary parameters for each command.

This I/O map defines the register addresses and functions for these I/O locations. For ease of reference, the commands are listed in alphabetical order.

Command:	Command Code								Parameters:				
	b7	b6	b5	b4	b3	b2	b1	b0	SC	SN	CY	DH	FR
Conner Specific	1	0	0	1	1	0	1	0	y	y	y	d	n
Execute Drive Diagnostic	1	0	0	1	0	0	0	0	n	n	n	d	n
Execute SMART Function	1	0	1	1	0	0	0	0	n	n	y	d	y
Format Track	0	1	0	1	x	x	x	x	n	n	y	y	n
Identify Device	1	1	1	0	1	1	0	0	n	n	n	d	n
Init. Device Parameters	1	0	0	1	0	0	0	1	y	n	n	y	n
Power Commands	1	1	1	0	0	p	p	p	y	n	n	d	n
Read DMA	1	1	0	0	1	0	0	r	y	y	y	y	n
Read Multiple	1	1	0	0	0	1	0	0	y	y	y	y	n
Read Sector(s)	0	0	1	0	0	0	L	r	y	y	y	y	n
Read Sector Buffer	1	1	1	0	0	1	0	0	e	n	e	d	n
Read Verify Sector(s)	0	1	0	0	0	0	0	r	y	y	y	y	n
Recalibrate	0	0	0	1	x	x	x	x	n	n	n	d	n
Seek	0	1	1	1	x	x	x	x	n	n	y	y	n
Set Features	1	1	1	0	1	1	1	1	n	n	n	d	y
Set Multiple Mode	1	1	0	0	0	1	1	0	y	n	n	d	n
Write DMA	1	1	0	0	1	0	1	r	y	y	y	y	n
Write Multiple	1	1	0	0	0	1	0	1	y	y	y	y	n
Write Sectors	0	0	1	1	0	0	L	r	y	y	y	y	n
Write Sector Buffer	1	1	1	0	1	0	0	0	e	n	e	d	n

where:

- **L** is the long bit, if 1, **R/W Long** commands are executed, if 0, normal R/W commands are performed.
- **r** is the retry bit; 0 = retries are enabled, 1 = retries are disabled. Retries that may be enabled/disabled are those on ECC and data errors. When retries are disabled at the start of a command, they are always automatically enabled at the end of the command.
- **SC** is the sector count register.
- **SN** is the sector number register.
- **CY** are the cylinder registers.
- **DH** is the device/head register.
- **FR** is the features (write precomp) register.
- **y** means the register contains a valid parameter for this command. For the device/head register, y means that both the drive and head parameters are used.
- **n** means the register does not contain a valid parameter for this command.

- **d** means only the drive parameter is valid and not the head parameter.
- **p** is a valid bit for power commands E0 - E3 and E5 - E6.
- **e** means the registers contain valid parameters when performing extended commands.
- **x** = don't care.

## **Command Register**

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All commands are decoded from the Command Register. The drive's host interface shall be programmed by the host computer to perform commands and will return status to the host at command completion.

To issue a command, the host must:

- load the pertinent registers in the Task File
- activate the interrupt enable bit, -IEN, in the Device Control register
- write the command code to the Command register

Execution begins as soon as the Command register is written.

The following sections describe the drive's supported command set. For ease of reference, the commands are listed in alphabetical order.

## Conner Specific

**Command Number:** 9A hex

**Description:** The Conner drive provides vendor-unique commands to allow for certain operations not provided by the standard command set. The Sector Number register must be set to 9A hex and the specific command in the Sector Count register. The Cylinder High and Low registers are used to pass any bytes used in a write operation.

The Conner specific command has the following decodes:

<i><b>Decode:</b></i>	<i><b>Description:</b></i>
<b>00 hex</b>	Get Feature Word
<b>01 hex</b>	Reserved
<b>02 hex</b>	Read drive switches
<b>03 hex</b>	Abort command
<b>04 hex</b>	Reserved
<b>05 hex</b>	Reserved
<b>06 hex</b>	Abort command
<b>07 hex</b>	Abort command
<b>08 hex *</b>	Power lock
<b>09 hex *</b>	Power unlock
<b>0A-FF hex</b>	Reserved

\* only valid on drives which implement Conner Power commands

The following sections describe these decodes in more detail.

**Get Drive Feature word (00)**

This command fetches the drive feature word and returns it in the Cylinder High and Cylinder Low registers. The bit meaning is as follows:

<b>Bit:</b>	<b>Description:</b>
15	Reserved
14	Reserved
13	Customer Reserved
12	Reserved
11	Reserved
10	Reserved
9	Reserved
8	ATA/CAM mode = 1
7	Reserved
6	Reserved
5	Reserved (enable no spin on POR)
4	Reserved
3	Disable Read Look Ahead Caching
2	Enable Write Caching
1	Customer Reserved
0	Customer Reserved

It is important to read the Feature word and then only change the bits of interest leaving the other bits unaffected using specific commands supported by this drive.

**Read the Drive Switches (02)**

This command returns the drive switches in the Cylinder Low Register. The bit meaning is as follows:

<b>Bit:</b>	<b>Description:</b>
7	Reserved
6	Reserved
5	-C/D
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

**Power Lock (08)**

This command prevents the drive from spinning down, and spins the drive up if the drive had been spun down.

**Power Unlock (09)**

This allows the drive to respond to the **Power** command and re-enables the power down time if applicable.

## Execute Drive Diagnostic

**Command Number:** 90 hex

**Description:** This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests are only executed upon receipt of this command.


The drive sets BSY immediately upon receipt of the command. If the drive is a master, the drive performs the diagnostic tests and saves the results. It then checks to see if a slave drive is present and waits up to 5 seconds for the slave to complete its diagnostics. If the slave successfully completes its diagnostics, it asserts -HOST PDIAG. If unsuccessful, the master drive resets BSY in the Status register and generates an interrupt. The Error bit (ERR) is set in the Status register and the Error register is updated.

The value in the Error register should be viewed as a unique 8-bit code and not as the single-bit flags defined previously. The interface registers are set to initial values except for the Error register.

The table below details the codes in the Error register and a corresponding explanation:

<b>Error Code:</b>	<b>Description:</b>
01 hex	No error detected
02 hex	Format device error
03 hex	Sector buffer error
8x hex	Slave drive failed

Additional codes may be implemented at the manufacturer's option.

 **Note:** If the slave drive fails diagnostics, the master drive shall "OR" 80 hex with its own status and load that code into the Error register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive shall set bit 7 of the Error register in the Task File to 0.

## Execute SMART Function

**Command Number:** B0 hex

This command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. There are several subcommands which are selectable via Features Register when the command is issued by the host.

The Cylinder Low and Cylinder High Registers must be written with the key values shown below prior to writing the command register or the command will terminate with the error bit set in the status register. Refer to the paragraph on

error reporting at the end of the description of this command for additional information regarding error reporting.

Any register is not specified as being written with a value by the host for this command is undefined and is ignored by the drive. The key values are shown below.

Key Value	Register
4F hex	Cylinder Low (1F4 hex)
C2 hex	Cylinder High (1F5 hex)

In order to select a subcommand the host must write the subcommand code to the drive's Features Register before issuing the Execute SMART Function command. The subcommands and their respective codes are listed below.

Code (hex)	Subcommand
<b>00-CF</b>	<b>Reserved</b>
<b>D0</b>	<b>Read Attribute Values</b> returns the drive's Attribute Values to the host. Upon receipt of the Read Attribute Values subcommand from the host, the drive asserts BSY, saves any updated Attribute Values to non-volatile memory, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the drive via the Data Register.
<b>D1</b>	<b>Read Attribute Thresholds</b> returns the drive's Attribute Thresholds to the host. Upon receipt of this subcommand from the host, the drive asserts BSY, reads the Attribute Thresholds from non-volatile memory, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Threshold information from the drive via the Data register.
<b>D2</b>	<b>Enable/Disable Attribute Autosave</b> subcommand is not implemented
<b>D3</b>	<b>Save Attribute Values</b> causes the drive to immediately save any updated Attribute Values to the drive's non-volatile memory. Upon receipt of this subcommand from the host, the drive asserts BSY, writes any updated Attribute Values to non-volatile memory, clears BSY and asserts INTRQ.
<b>D4 - D6</b>	<b>Reserved</b>
<b>D7</b>	<b>Vendor Specific</b>

Code (hex)	Subcommand
<b>D8</b>	<p><b>Enable SMART Operations</b> enables access to all SMART capabilities within the drive. Prior to receipt of an Enable Smart Operations subcommand Attribute Values are neither monitored nor saved by the drive. The state of SMART (either enabled or disabled) will be preserved by the drive across power cycles. Once enabled, the receipt of subsequent Enable Smart Operations subcommands shall not affect any of the Attribute Values.</p> <p>Upon receipt of this subcommand from the host, the drive asserts BSY, enables SMART capabilities and functions, clears BSY and asserts INTRQ.</p>
<b>D9</b>	<p><b>Disable SMART Operations</b> This subcommand disables all SMART capabilities within the drive. After receipt of the Disable Smart Operations subcommand the drive will disable all SMART operations. Attribute Values will no longer be monitored or saved by the drive. The state of SMART (either enabled or disabled) will be preserved by the drive across power cycles.</p> <p>Upon receipt of the Disable Smart Operations subcommand from the host, the drive asserts BSY, disables SMART capabilities and functions, clears BSY and asserts INTRQ.</p> <p>After receipt by the drive of the Disable Smart Operations subcommand from the host, all other SMART subcommands with the exception of Enable Smart Operations subcommand are disabled and invalid. They will be aborted by the drive (including the Disable Smart Operations subcommand), returning the error code specified at the end of this command description.</p> <p>Any Attribute Values accumulated and saved to non-volatile memory prior to receipt of the Disable Smart Operations command will be preserved in the drive's non-volatile memory. If the drive is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a Read Attribute Values or Save Attribute Values command.</p>
<b>DA</b>	<b>Return SMART Status</b> is not implemented
<b>DB - DF</b>	<b>Reserved</b>
<b>E0 - EF</b>	<b>Vendor Specific</b>

### ***Device Attributes Data Structure***

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the Read Attribute Values subcommand. All multi-byte fields shown in these data structures follow the ATA-2 convention for byte ordering, i.e., the least significant byte occupies the lowest numbered byte address location in the field.

**Table 7-1 - Device Attributes Data Structure**

<b>Description</b>	<b>Bytes</b>	<b>Format</b>	<b>Type</b>
Data Structure Revision Number = 0004 hex	2	binary	Rd only
1 <sup>st</sup> Device Attribute	12	see below	Rd/Wrt
..			
..			
..			
30 <sup>th</sup> Device Attribute	12	see below	Rd/Wrt
Reserved (00 hex)	6		Rd only
SMART Capability = 0000H	2		Rd only
Reserved (00 hex)	16		Rd/Wrt
Vendor Specific	125		Rd only
Data Structure Checksum	1		Rd only
Total Bytes	512		

**Data Structure Revision Number**

The Data Structure Revision Number identifies which version of this data structure is implemented by the drive. The CFS635A/850A/1275A supports SMART revision 4.0.

### Individual Attribute Data Structure

The following defines the twelve bytes that make up the information for each Attribute entry in the Device Attributes Data Structure.

**Table 7-2 - Individual Attribute Data Structure**

Description	Bytes	Format	Type
Attribute ID Number (01 hex to FF hex)	1	binary	Rd only
Status Flags	2	bit flags	Rd only
Pre-Failure/Advisory bit			
Vendor Specific (5 bits)			
Reserved (10 bits)			
Attribute Value (valid values from 01 hex to FE hex)	1	binary	Rd only
00 hex: invalid for Attribute value- not to be used			
01 hex: minimum value			
64 hex: initial value for all attributes prior to any data collection			
FD hex: maximum value			
FE hex: value is not valid.			
FF hex: invalid for Attribute value not to be used			
Vendor Specific	8	binary	Rd only
Total Bytes	12		

### Attribute ID Numbers

The Attribute ID Numbers and their definitions are shown below. Any non-zero value in the Attribute ID Number indicates an active attribute. Valid values for this byte are from 01 hex through FF hex.

Attribute ID	Description
1	Firm error rate
3	Spin up time
4	Spin up count
5	Retired sectors
7	Seek error rate
10	Spin retries
12	Drive power cycle count

### Status Flags

The following describes the definitions for the Status Flags:

bit	hex value	Description
0	0001	<b>Pre-Failure/Advisory Bit</b> when = 0 means an Attribute Value less than or equal to its corresponding Attribute Threshold is indicating an advisory condition where the usage or age of the drive has exceeded its intended design life period.  When = 1 means that an Attribute Value less than or equal to its corresponding Attribute Threshold is indicating a Pre-Failure condition where imminent loss of data is being predicted.
1	0002	<b>Reserved</b>
2	0004	<b>Vendor Specific</b>
3	0008	<b>Vendor Specific</b>
4	0010	<b>Vendor Specific</b>
5	0020	<b>Vendor Specific</b>
6-F	0040-8000	<b>Reserved</b>

### Attribute Values

The range and meaning of the Attribute Values is defined in Table 7-2. Prior to the monitoring and saving of Attribute Values, all values are set to 64 hex. The Attribute Values of 00 hex and FF hex are reserved and should not be used by the drive.

### SMART Capability

This word of bit flags describes the SMART capabilities of the drive. This word is equal to 0000 for this drive.

bit	hex value	Description
0	0001	<b>Pre-Power Mode Attribute Saving Capability Bit</b> , when = 1, means the drive will save its Attribute Values prior to going into a power saving mode (Idle, Standby or Sleep modes.)
1	0002	<b>Attribute AutoSave After Event Capability Bit</b> when = 1, means that the drive supports the Enable/Disable Attribute Autosave subcommand.
2-F	0004-8000	<b>Reserved</b> for future use

### Data Structure Checksum

The Data Structure Checksum is the two's complement of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

### Device Attribute Thresholds Data Structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the Read Attribute Thresholds subcommand. All multi-byte fields shown in these data structures follow the ATA-2 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds must appear in the same order as their corresponding Attribute Values.

**Table 7-3 - Device Attribute Thresholds Data Structure**

Description	Bytes	Format	Type
Data Structure Revision Number = 0004 hex	2	binary	Rd only
1 <sup>st</sup> Device Attribute Threshold	12	see below	Rd/Wrt
..			
..			
..			
30 <sup>th</sup> Device Attribute	12	see below	Rd/Wrt
Reserved (00 hex)	18		Rd only
Vendor Specific	131		Rd only
Data Structure Checksum	1		Rd only
Total Bytes	512		

### Data Structure Revision Number

This value will be the same as the value used in the Device Attributes Values Data Structure.

### Individual Threshold Data Structure

The following defines the twelve bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure must be in the same order and correspond to the entries in the Individual Attribute Data Structure.

**Table 7-4 - Individual Threshold Data Structure**

Description	Bytes	Format	Type
Attribute ID Number	1	binary	Rd only
Attribute Threshold (for comparison with Attribute values from 00 hex to FF hex)	1	binary	Rd only
00 hex: "always passing" threshold value to be used for code test purposes			
01 hex: minimum value for normal operation			
64 hex: maximum value for normal operation			
FD hex: maximum value			
FE hex: invalid for threshold value-not to be used.			
FF hex: "always failing" threshold value to be used for code test purposes			
Reserved	10	binary	Rd only
Total Bytes	12		

### Attribute ID Numbers

The Attribute ID Numbers must match the ID numbers in the Attribute Data Structure. Any non-zero value in the Attribute ID Number indicates an active attribute.

### Attribute Threshold

These values are set at the factory and are not changeable in the field.

### Data Structure Checksum

The Data Structure Checksum is the two's compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

### **Error Reporting**

The Execute SMART Function command will terminate with an aborted command error condition under the following circumstances:

- The required key values were not loaded into the Cylinder High and Cylinder Low registers.
- An invalid or not supported subcommand code in the Features Register.
- The command is received by the drive while the drive was in a "SMART disabled" state.
- The drive is unable to read its Attribute Values or Attribute Threshold data structure
- The drive is unable to write to its Attribute Values data structure.

The meaning of the following bits in the Error register do not correspond the definitions found in the description of the Error register:

<b>bit</b>	<b>Value (Hex)</b>	<b>Description</b>
0	01	The Data Structure Revision Number in the drive's Attribute Values data structure does not match the Data Structure Revision Number in the drive's Attribute Thresholds data structure.  A mismatch has occurred between the entries in the drive's Attribute Values data structure and Attribute Thresholds data structure.
4	10	The drive has detected a checksum error in its Attribute Threshold data structure.

## Format Track

**Command Number:** 50 hex

**Description:** This command provides a means by which a defective sector may either be marked bad or reassigned. This command has been used on other drives to do the low level formatting job of putting the header and creating the data fields for all tracks on the drive.

It is not necessary to execute a **Format** command prior to operating the drive on the host PC because the drive is a hard-sectored drive and all required low-level formatting is done when built. Conner supports the **Format** command only to allow any sectors that become defective to be handled in a fashion required by different operating systems. It should be noted that the **Format** command operates on one single logical track at a time and that all sectors on that track are filled with zeroes.

There are two methods provided to handle defective sectors.

### **Marked Bad Sector**

When a sector is marked bad, the ID field of the sector is updated to indicate a bad block. Any time that sector is accessed thereafter, the drive will return bad block status in the Error register. It is also possible to format a bad block good and use sectors previously formatted bad. The total capacity of the drive is reduced when sector is formatted bad.

### **Assign**

The second method, Assign, allows a spare sector on the drive to be used to replace the specified sector. Following this operation, the drive performance will be degraded slightly when the sector is accessed due to the drive automatically going to the new sector. It is also possible to unassign an alternate. When a sector or sectors on a single track are unassigned, the first spare sector is the only one recoverable. Creating a diagnostic routine that performs large scale assign and unassign is not recommended.

The **Format Track** command is like a **Write** command, i.e., the Task File is written, the Command register is written to begin the command, and the drive responds by activating DRQ in the Status register. This indicates a request for 1 sectors (512 bytes) worth of data that is used to describe the operations to be performed on each sector of the track specified by the Task File. After the data is written to the Data register, the drive analyzes the information for each sector and performs the requested action to each sector. When the command is complete, the drive raises Interrupt Request with ending status in the Task File.

The data in the sector buffer must conform to a specified format. There must be one word, two bytes, for each sector. The words must be contiguous and begin at the start of the sector. Unlike some drives where the order of the words is used to determine the interleave, the order of the words is not significant because the drive's interleave cannot be changed. The MSB of each word must contain the

sector number. The LSB must contain a descriptor byte that indicates what is to be done to each sector. There are four possible descriptor bytes:

- 00 hex = format sector good
- 80 hex = format sector bad
- 40 hex = assign this sector to an alternate location
- 20 hex = unassign the alternate location for this sector

The drive will return an ID not found under any of the following conditions:

- There is a missing word for any sector along the track.
- The words are not contiguous from the start of the sector.
- There is more than one (1) word per sector.
- The Task File calls for an illegal cylinder and/or head register.

A utility program to handle defective sectors should provide some interface to obtain the defective sectors. The program should build a 512 byte block with a word for each sector for the track. These words must be in the first contiguous words of the block. The MSB of each block should contain the sector number. Then the defective sectors descriptor byte should be set to either 80 hex or 40 hex, depending on whether or not the sector is to be formatted bad or reassigned. All the remaining sectors should have a descriptor byte of 0 hex, which means to format the sector good. Once the data byte block is created, the **Format** command can be executed by interfacing it to the BIOS.

It is important to remember that all data on the track is lost. The drive formats to the logical track that is the power-on reset default, or to the values issued by the last **Initialize Device Parameters** command.

## Identify Device

**Command Number:** EC hex

**Description:** This command allows the host to receive parameter information from the drive.

When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The host may then read the information out of the sector buffer.

The parameter words in the buffer are arranged as follows. All reserved bits or words should be zeroes. All numbers are given in hexadecimal format, right-justified.

<b>Word (hex):</b>	<b>Description:</b>
0	General configuration bit significant information (0C5A)
1	Default number of cylinders
2	Number of removable cylinders
3	Default number of heads
4	Number of unformatted bytes per logical track
5	Number of bytes per sector
6	Default number of sectors per track
7	Number of bytes in the inter-sector gaps
8	Number of bytes in the Sync fields
9	0000
10-19	Serial number right justification
20	Controller type 0003 dual-ported multiple sector buffer with Look Ahead Read
21	Controller buffer size in 512-byte increments
22	Number of ECC bytes on R/W long commands
23-26	Controller firmware revision
27-46	Model number
47	Number of sectors per interrupt on Multiple commands: <ul style="list-style-type: none"> <li>• bits 15-8: 80 hex</li> <li>• bits 7-0: 00 hex means Read/Write multiple not implemented; xx hex is the maximum number of sectors that can be transferred per multiple command</li> </ul>
48	Double word transfer flag. 0 = not capable, 1 = capable

<b>Word (hex):</b>	<b>Description:</b>
<b>49</b>	Capabilities definitions bits 15-12 0 = (reserved) bit 11 1 = IORDY supported bit 10 1 = IORDY can be disabled bit 9 1 = LBA supported bits 8 1 = DMA supported bits 7-1 0 = (reserved) bits 0 1 = assign alternate supported
<b>50</b>	Modes supported
<b>51</b>	bits 15-8 PIO data transfer cycle timing mode bits 7-0 vendor unique
<b>52</b>	bits 15-8 = DMA data transfer timing mode
<b>53</b>	bits 15-2 Reserved bit 1 1 = the fields reported in words 64-70 are valid 0 = the fields reported in words 64-70 are not valid bit 0 1 = the fields reported in words 54-58 are valid 0 = the fields reported in words 54-58 are not valid
<b>54</b>	Number of current logical cylinders
<b>55</b>	Number of current logical heads
<b>56</b>	Number of current sectors per logical track
<b>57</b>	LSW Current capacity in sectors
<b>58</b>	MSW Current capacity in sectors
<b>59</b>	bits 15-9 Reserved bit 8 1 = Multiple sector setting is valid bits 7-0 xx = current setting for number of sectors per transfer in multiple mode
<b>60</b>	LSW Total number of user addressable sectors (LBA mode only)
<b>61</b>	MSW Total number of user addressable sectors (LBA mode only)
<b>62</b>	bits 15-8 Single word DMA transfer mode active bits 7-0 Single word DMA transfer mode supported
<b>63</b>	bits 15-8 01 hex = Multiword DMA transfer mode active bits 7-2 reserved for future Multiword DMA transfer modes** bit 1 1 = Multiword DMA transfer Mode 1 supported 0 = Multiword DMA transfer Mode 1 NOT supported bit 0 1 = Multiword DMA transfer Mode 0 supported 0 = Multiword DMA transfer Mode 0 NOT supported
<b>64</b>	bits 15-8 Reserved bits 7-2 reserved for future Advanced PIO Modes*** bit 1 1 = PIO Mode 4 supported 0 = PIO Mode 4 not supported bit 0 1 = PIO Mode 3 supported 0 = PIO Mode 3 not supported

<b>Word (hex):</b>	<b>Description:</b>
<b>65</b>	Minimum multiword DMA transfer cycle time per word (ns)
<b>66</b>	Recommended multiword DMA transfer cycle time (ns)
<b>67</b>	Minimum PIO transfer cycle time without flow control (ns)
<b>68</b>	Minimum PIO transfer cycle time with IORDY flow control (ns)
<b>69-127</b>	Reserved
<b>128</b>	Native number of Cylinders
<b>129</b>	Native number of Heads   Sectors
<b>130</b>	Current logical number of Cylinders
<b>131</b>	Current logical number of Heads   Sectors
<b>132</b>	Feature Word
<b>133</b>	Power commands supported (FFFF if supported)
<b>134</b>	bit 15-2: reserved bit 1: ATA/CAM compliant bit 0: 1= current logical numbers, 0 = default logical numbers
<b>135</b>	MSB = drive age LSB = drive program
<b>136-255</b>	Reserved

*	<b>Mode 0</b>	<b>Mode 1</b>	<b>Mode 2</b>
<b>PIO Timing Parameters</b>	<b>(nsec)</b>	<b>(nsec)</b>	<b>(nsec)</b>
<b>Cycle Time</b>	600	383	240
**	<b>Mode 0</b>	<b>Mode 1</b>	
<b>Multiword DMA Timing</b>	<b>(nsec)</b>	<b>(nsec)</b>	
<b>Cycle Time</b>	480	>= 150	
***			<b>Mode 3</b>
<b>Advanced PIO Timing</b>			<b>(nsec)</b>
<b>Cycle Time</b>			>= 180

## ***Initialize Device Parameters***

**Command Number:** 91 hex

**Description:** This command enables the host to set the head switch and cylinder increment points for multiple sector operations.

In the Translate mode, the logical head and sector numbers in the Task File will be translated to their native physical values as part of execution of the command.

The sector and head values in the Task File are not checked for validity by this command. If they are invalid, no error will be reported until an illegal access is made by some other command. Cylinder head increments on subsequent commands will occur after access of the maximum sector and maximum head specified by this command. Upon receipt of the command, the drive sets BSY, saves the parameters, resets BSY, and generates an interrupt.

Conner has established a Universal Translate Mode which enables the you to configure the drive in an AT environment to any cylinder, head, and sector configuration desired (refer to chapter 3).


## Power Commands

**Command Number:** Ex hex

**Description:** The **Power** commands are supported on some Conner drives, including the CFS635A/CFS850A/CFS1275A. If a **Power** command is issued to a drive that does not support the **Power** commands, an Abort status will be returned to the host in the Error register.

Commands E0 through E3 and E5-E6 constitute the **Power** commands. The following table describes these commands:

<i>Error Code:</i>	<i>Description:</i>
<b>E0 hex</b>	The drive enters Standby Mode immediately
<b>E1 hex</b>	The drive enters Idle Mode immediately
<b>E2 hex</b>	The drive enters Standby Mode immediately.  If the Sector Count register is non-zero, then the Auto Power-Down feature is enabled and will take effect when the drive returns to Idle Mode.  If the Sector Count register is zero, then the Auto Power-Down feature is disabled.
<b>E3 hex</b>	The drive enters Idle Mode immediately.  If the Sector Count register is non-zero, then the Auto Power-Down feature is enabled and will take effect immediately.  If the Sector Count register is zero, then the Auto Power-Down feature is disabled.
<b>E5 hex</b>	Puts FF hex in the Sector Count register if the drive is in Idle Mode.  Puts 00 hex in the Sector Count register if the drive is in, going to, or recovering from the Standby Mode.  Puts BB hex in the Sector Count register if power lock is enabled.
<b>E6 hex</b>	The drive enters Sleep Mode. A reset is required to bring the drive out of Sleep Mode.

 **Note:** Minimum power off/on cycle time is 60 seconds.

All of the **Power** commands except command E6 will execute immediately and return the ending interrupt after the spin up/down sequence is initiated. Please note that if the drive is already spinning (Idle Mode) and a spin-up command is issued from the host, the spin-up sequence is not initiated.

Similarly, if the drive is in Standby Mode and the host issues a spin-down command, the spin-down sequence is not initiated.

Return of the ending interrupt does not mean that the drive has fully transitioned to the desired operating mode. The Sleep command is the exception. In command E6, the drive is spun down and when it is stopped, the drive returns the ending interrupt and the Sleep Mode begins.

When enabling the Auto Power-Down feature, the value in the Sector Count register specifies the number of 5-second increments for the time-out value. If the drive does not receive a command within the specified time, the drive will enter Standby Mode. The minimum time-out value is 60 seconds, which means the smallest value for the Sector Count register is 12 when enabling the Auto Power-down feature. If a number between 1 and 11 inclusive is specified in the Sector Count register, a value of 12 is used. This prevents overheating of the drive during spin-up/down sequences.

Assertion of Host Reset will only affect the current state of the Sleep Mode. If the drive is in Sleep Mode and Host Reset is asserted, the drive wakes up into Standby Mode. Please note that the drive will not return to the state it was in when the host issued the Sleep command. The default power-on condition of the drive is Idle Mode.

## Read DMA

**Command Number:** Cx hex

**Description:** This command enables the controller to do EISA Type B Demand Mode DMA reads. These are two versions of this command, as shown below:

<b>Command Number:</b>	<b>Command Name</b>
C8 hex	DMA Read with retries
C9 hex	DMA Read without retries

When the command is received, the drive will go busy and read the data into the buffer from the disk. When a sector is in the buffer, the drive will go not busy and activate Host DMA Request to initiate the transfer. The drive will then place data on the Host Data Bus whenever the host activates -Host IOR and -Host DMA ACK.

The drive will leave Host DMA Request active as long as there is data to transfer. When waiting for more data to be placed in the buffer, the drive will inactivate Host DMA Request until there is enough data in the buffer to transfer

again. When the transfer is complete, the drive will become busy, verify no errors, and then go not busy and activate the Host IRQ line.

If the command is performed with the retries disabled bit active retries will be disabled.

## **Read Multiple**

**Command Number:** C4 hex

**Description:** This command is identical to the **Read Sector** operation but several sectors are transferred to the host as a block without intervening interrupts and only requiring DRQ qualification of the transfer on the first sector of the block of sectors to be transferred. Long transfers are not permitted.

The block count, which is the number of sectors to be transferred as a block, is programmed by the **Set Multiple** mode command which must be executed prior to the **Read Multiple** command. When the **Read Multiple** command is issued, the Sector Count register will contain the number of sectors (not the number of blocks or the block count) requested.

If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where:

$$N = (\text{sector count}) \bmod (\text{block count})$$

If the **Read Multiple** command is attempted before the **Set Multiple** mode command has been executed or when multiple commands are disabled, the multiple operation will be rejected with an Aborted Command Error.

Disk errors encountered during multiple commands will be reported at the beginning of the block or partial block transfer, but DRQ will still be set and the transfer will take place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks will only be transferred if the error was a correctable data error. All other errors will cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

## Read Sector(s)

**Command Number:** 2x hex

**Description:** This command will read from 1 to 256 sectors as specified in the Task File (a sector count of 0 is a request for 256 sectors), beginning at the specified sector. There are four versions of this command, as shown below:

<i>Command Number:</i>	<i>Command Name</i>
20 hex	Read with retries
21 hex	Read without retries
22 hex	Read long with retries
23 hex	Read long without retries

As soon as the Command register is written, the drive sets the BSY bit and begins execution of the command.

Upon execution, the Error bit (ERR) is set in the Status register and the Error register is updated. Also:

- If bits 2 and 3 of the Command register are not equal to zero, then the Aborted Command bit (ABRT) is set.
- If incorrect Task File parameters are passed, the ID Not Found Error (IDNF) is set.

If the drive is not already on the desired track, an implied **Seek** is performed. Once at the desired track, the drive begins searching for the appropriate ID field.

- If the ID is read correctly, the data field is read into the sector buffer.
- Error Bits are set if an error was encountered.

The DRQ bit is set and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector. Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector reads set DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector and the drive is ready for the data to be transferred to the host. DRQ is reset and BSY is set immediately after the host empties the sector buffer.

If no error is detected, the cylinder, head, and sector registers are updated to point to the next sequential sector.

If either a correctable data error or a non-correctable data error occurs, the flawed data is loaded into the sector buffer.

- The read does not terminate if the error was a correctable data error.
- If a non-correctable data error occurs during a multiple sector read, the read will terminate at the sector where the error occurs. The Task File Registers will contain the cylinder, head, and sector number of the sector where the error occurred. The host may then read the Task File to determine what error has occurred, and on which sector.

A **Read Long** may be executed by setting the long bit in command code. The **Read Long** command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine there has been any type of data error. Data bytes are 16-bit transfers and ECC bytes are 8-bit transfers.

## ***Read Sector Buffer***

**Command Number:** E4 hex

**Description:** The **Read Buffer** command allows the host to read the current contents of the drive's sector buffer. Only the Command register is valid for this command.

When this command is issued, the drive will set BSY, set up the sector buffer for a read operation, set DRQ, reset BSY, and generate an interrupt. The host may then read up to 512 bytes of data from the buffer.

An option provided by Conner is to perform an extended **Read Buffer** command. If 599A hex is placed in the Cylinder register, then the Sector Count register is used to pass that many sectors out of the buffer. If the requested sector count is larger than the buffer, an Aborted Command error status is returned.

## Read Verify Sectors

**Command Number:** 4x hex

**Description:** This command functions similarly to the **Read Sectors** command, except that no data is transferred to the host and at completion of the command. There are two versions of this command, as shown below:

<b>Command Number:</b>	<b>Command Name</b>
40 hex	Read Verify with retries
41 hex	Read Verify without retries

The CORR bit is set if software ECC correction was required. The drive remains Busy until all data is verified. If Look Ahead Read is active, the **Verify** command will also work the same as when a **Read** is performed.

## Recalibrate

**Command Number:** 10 hex

**Description:** This command will move the read/write heads from anywhere on the disk to cylinder 0.

Upon receipt of the command, the drive sets BSY, resets DSC, and executes a **Seek** to cylinder zero. The drive then waits for the **Seek** to complete before updating status, resetting BSY, setting DSC, and generating an interrupt.

If the drive cannot reach cylinder 0, the Error Bit (ERR) is set in the Status register and the track 0 (TK0) bit is set in the Error register.

If the drive is not spinning or is not on track, an aborted command (ABRT) response will be given in the Error register.

Upon successful completion of the command, the Task File registers will be as follows:

<b>Register:</b>	<b>Value:</b>
Error	00
Sector Count	Unchanged
Sector Number	Unchanged
Cylinder Low	00
Cylinder High	00
Device/Head	Unchanged

## Seek

**Command Number:** 70 hex

**Description:** This command initiates a **Seek** to the track and selects the head specified in the Task File.

When the command is issued, the drive sets BSY in the Status register, resets Seek Complete (DSC), initiates the **Seek**, resets BSY, and generates an interrupt. Only the Cylinder register and Drive Head register are valid for this command.

The drive does not wait for the **Seek** to complete before returning the interrupt. Seek Complete (DSC) will be set upon completion of the command.

If a new command is issued to a drive while a **Seek** is being executed, the drive will wait, with BSY active, for the **Seek** to complete before executing the new command. No checks are made on the validity of the Sector number in the Task File. The Error Bit (ERR) in the Status register and the ID Not Found (IDNF) bit in the Error register of the Task File will be set if an illegal cylinder number is passed.

## Set Features (Set Look Ahead Read)

**Command Number:** EF hex

**Description:** This command is used by the host to establish the following parameters which affect the execution of certain drive features as shown below:

- 02 hex enables write cache.
- 82 hex disables write cache.
- AA hex enables Read Look Ahead.
- 55 hex disables Read Look Ahead.
- 03 Set Transfer Mode

Any other values in the Features (Write Precompensation) register will result in the Error bit set in the Status Register and the ABRT (abort) bit set in the Error Register. The default state on power up (Power On Reset) is determined by the value of the Feature Word, which is factory set. The drive will retain the settings through both soft and hard resets.

The Set Transfer Mode command set the current transfer mode according to the content of the Sector Count Register. The valid Sector Count Register values are shown in the table below:

<i>Sector Count Register</i>	<i>Transfer Mode</i>
00 hex	Set default PIO transfer mode
01 hex	Disable IOCHRDY
08 hex	Enable Mode 0 PIO with IOCHRDY enabled
09 hex	Enable Mode 1 PIO with IOCHRDY enabled
0A hex	Enable Mode 2 PIO with IOCHRDY enabled
0B hex	Enable Mode 3 PIO with IOCHRDY enabled
0C hex	Enable Mode 4 PIO with IOCHRDY enabled
20 hex	Enable Multiword DMA Mode 0
21 hex	Enable Multiword DMA Mode 1
22 hex	Enable Multiword DMA Mode 2

One transfer mode subcommand may be issued for each SET FEATURES Command.

## Set Multiple Mode

**Command Number:** C6 hex

**Description:** This command enables the controller to perform **Read Multiple** and **Write Multiple** operations and establishes the block count for these commands. Prior to command issuance, the Sector Count register should be loaded with the number of sectors per block. Block counts supported are multiples of 2 up to the buffer size of each drive, e.g. 1,2,4,8.

Upon receipt of the command, the controller sets BSY and looks at the Sector Count register contents. If the register contents are valid and a supported block count is supplied, that value is loaded for all subsequent **Read Multiple** and **Write Multiple** commands and execution of these commands is enabled. Any unsupported block count in the register will result in an Aborted Command Error and any **Read Multiple** and **Write Multiple** commands will be disabled.

If the Sector Count register contains 0 when the command is issued, any **Read Multiple** and **Write Multiple** commands will be disabled. Once the appropriate action has been taken, the controller resets BSY and generates an interrupt. At power-up the default is for **Read Multiple** and **Write Multiple** to be disabled.

The state of **Read Multiple** and **Write Multiple** is maintained through both hardware and software resets when the drive is in ISA/Conner mode.

## Write DMA

**Command Number:** Cx hex

**Description:** This command allows the drive to perform write operations using EISA DMA Demand Type B transfers. These are two versions of this command, as shown below:

<b>Command Number:</b>	<b>Command Name</b>
<b>CA hex</b>	DMA Write with retries
<b>CB hex</b>	DMA Write without retries

When the command is received, the drive will go busy and activate Host DMA Request. The drive will then accept data into its Data register whenever the host activates both -Host IOW and -Host DMACK. Host DMA Request will remain active until all data has been transferred.

Following the completion of the data transfer, the drive will go busy. When all the data is on the disk and the operation is complete, the drive will go not busy and activate Host IRQ.

If the command is performed with the retries disabled bit active, retries will be disabled.

### **Write Caching**

Write caching is activated by setting the Feature Word bit 2. Once write caching is active, the **Write DMA** command is cached. This command is then referred to as a “cached write.”

When a cached write command is received, the data is taken from the host and ending status is posted before the data has been written to the disk.

- If the next command is a cached write and the data is logically sequential, the data is taken from the host immediately.
- If the next command is a cached write that is **not** logically sequential, the drive will wait for the previous write to finish before taking the data from the new write. Read commands work similarly; the previous write is allowed to finish before the read operation starts.

In addition to caching, dynamic sparing of bad sectors has been implemented for cached write commands. This ensures that cached data that has already been reported as written successfully gets written, even if an error should occur.

If a sector cannot be written, the drive will dynamically assign an alternate sector and continue writing the data. A limit of 100 spares has been set and if reached, the drive will drop out of write caching and report the error as an ID Not Found. If the write command is still active on the AT interface, the error is reported during that command; otherwise, it is reported on the next command.

## Write Multiple

**Command Number:** C5 hex

**Description:** This command performs similarly to the **Write Sector** command except that the controller sets BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Several sectors are transferred to the host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block, not on each sector. There is no IRQ prior to the first block transfer.

The block count, which is the number of sectors to be transferred as a block, is programmed by the **Set Multiple** mode command, which must be executed prior to the **Write Multiple** command. When the **Write Multiple** command is issued, the Sector Count register will contain the number of sectors (not the number of blocks or the block count) requested.

If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where:

$$N = (\text{sector count}) \bmod (\text{block count})$$

If the **Write Multiple** command is attempted before the **Set Multiple** mode command has been executed or when **Write Multiple** commands are disabled, the **Write Multiple** operation will be rejected with an Aborted Command Error.

All disk errors encountered during **Write Multiple** commands will be reported after the attempted disk write of the block or partial block is transferred. The write operation will end with the sector in error, even if it was in the middle of a block. Subsequent blocks will not be transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

### Write Caching

Write caching is activated by setting the Feature Word bit 2. Once write caching is active, the **Write Multiple** command is cached. This command is then referred to as a “cached write.”

When a cached write command is received, the data is taken from the host and ending status is posted before the data has been written to the disk.

- If the next command is a cached write and the data is logically sequential, the data is taken from the host immediately.
- If the next command is a cached write that is **not** logically sequential, the drive will wait for the previous write to finish before taking the data from the new write. Read commands work similarly; the previous write is allowed to finish before the read operation starts.

In addition to caching, dynamic sparing of bad sectors has been implemented for cached write commands. This ensures that cached data that has already been reported as written successfully gets written, even if an error should occur.

If a sector cannot be written, the drive will dynamically assign an alternate sector and continue writing the data. A limit of 100 spares has been set and if reached, the drive will drop out of write caching and report the error as an ID Not Found. If the write command is still active on the AT interface, the error is reported during that command; otherwise, it is reported on the next command.

## Write Sector(s)

**Command Number:** 3x hex

**Description:** This command will write from 1 to 256 sectors as specified in the Task File (a sector count of 0 is a request for 256 sectors), beginning at the specified sector. There are four versions of this command, as shown below:

<b>Command Number:</b>	<b>Command Name</b>
<b>30 hex</b>	Write with retries
<b>31 hex</b>	Write without retries
<b>32 hex</b>	Write long with retries
<b>33 hex</b>	Write long without retries

As soon as the Command register is written, the drive waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive sets BSY and begins command execution.

- If bits 2 and 3 of the Command register are on, the command terminates with Aborted Command.
- If incorrect task file parameters are passed, an H ID Not Found error is returned.

If the drive is not already on the desired track, an implied **Seek** is performed. Once at the desired track, the drive begins searching for the appropriate ID field.

- If the ID is correct, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes.
- Error bits are set if an error was encountered.

Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector written. The sector count is zero after successful execution of the command.

Multiple sector writes set DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is reset and BSY is set immediately when the host fills the sector buffer.

If no error is detected, the cylinder, head, and sector registers are updated to point at the next sequential sector.

If an error occurs during a multiple sector write, it will terminate at the sector where the error occurs. The Task File indicates the location of the sector where the error occurred. The host may then read the Task File to determine what error has occurred, and on which sector.

A **Write Long** may be executed by setting the long bit in the command code. The **Write Long** command writes the data and the ECC bytes directly from the sector buffer; the drive will not generate the ECC bytes itself for the **Write Long** command. Data byte transfers are 16-bit transfers and ECC bytes are 8-bit transfers.

### **Write Caching**

Write caching is activated by setting the Feature Word bit 2. Once write caching is active, the **Write Sector(s)** command is cached. This command is then referred to as a “cached write.”

When a cached write command is received, the data is taken from the host and ending status is posted before the data has been written to the disk.

- If the next command is a cached write and the data is logically sequential, the data is taken from the host immediately.
- If the next command is a cached write that is **not** logically sequential, the drive will wait for the previous write to finish before taking data from the new write. Read commands work similarly; the previous write is allowed to finish before the read operation starts.

In addition to caching, dynamic sparing of bad sectors has been implemented for cached write commands. This ensures that cached data that has already been reported as written successfully gets written, even if an error should occur.

If a sector cannot be written, the drive will dynamically assign an alternate sector and continue writing the data. A limit of 100 spares has been set and if reached, the drive will drop out of write caching and report the error as an ID Not Found. If the write command is still active on the AT interface, the error is reported during that command; otherwise, it is reported on the next command.

## **Write Sector Buffer**

**Command Number:** E8 hex

**Description:** The **Write Buffer** command allows the host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the Command register is valid for this command.

When this command is issued, the drive will set BSY, set up the sector buffer for a write operation, set DRQ, reset BSY. The host may then write up to 512 bytes of data to the buffer.

An option provided by Conner is to perform an extended **Write Buffer** command. If 599A hex is placed in the Cylinder Register, the Sector Count register is used to determine how many sectors will be written. If the Sector Count is larger than the buffer, an Aborted Command error status is returned.



## Error and Status Detection

In general, status and errors are detected in the following fashion by the drive microprocessor.

At the start of the execution of the command, the command register is checked for conditions that would lead to an aborted command. If an error is found, an error message is returned in the error register. Otherwise, the operation is attempted.

If the operation is attempted and fails, a message is returned. Any error terminates the command at the point that it is discovered.

## Error and Status Messages

The error and status bits that are valid for each command are summarized below. When BSY=1, all other bits in the Status register are not valid. The bits in the Error register are valid only when ERR is set in the Status Register and BSY=0. The definitions of each of these messages are found in chapter 6.

<b>Command</b>	<b>Valid Bits in Status Register</b>	<b>Valid Bits in Error Register</b>
Execute Drive Diag.	ERR	Refer to command description in Ch 7.
Execute SMART Func.	DRDY, DWF, DSC, ERR	ABRT, IDNF
Format Track	DRDY, DWF, DSC, ERR	ABRT, IDNF
Identify Device	ERR	ABRT
Init Device Parameters	ERR	ABRT
Power Commands	ERR	ABRT
Read Buffer	ERR	ABRT
Read Long	DRDY, DWF, DSC, ERR	BBK, IDNF, ABRT
Read Multiple	DRDY, DWF, DSC, CORR, ERR	BBK, UNC, IDNF, ABRT
Read Sector(s)	DRDY, DWF, DSC, CORR, ERR	BBK, UNC, IDNF, ABRT
Recalibrate	DRDY, DSC, ERR	ABRT, TKO
Seek	DRDY, DSC, ERR	IDNF, ABRT
Set Features	ERR	ABRT

<b>Command</b>	<b>Valid Bits in Status Register</b>	<b>Valid Bits in Error Register</b>
Set Multiple	ERR	ABRT
Write Buffer	ERR	ABRT
Write Multiple	DRDY, DWF, DSC, ERR	BBK, IDNF, ABRT
Write Sector(s)	DRDY, DWF, DSC, ERR	BBK, IDNF, ABRT
Write Long	DRDY, DWF, DSC, ERR	BBK, IDNF, ABRT
Verify Sectors	DRDY, DWF, DSC, CORR, ERR	BBK, UNC, IDNF, ABRT
Invalid Command Code	ERR	ABRT

Revision		Description	Date
Previous	Current		
Preliminary, Release I March 1995	Preliminary Release I June 1995	<ul style="list-style-type: none"><li>• Added CFS635A (p1, 3, 8,13, 16, 58)</li><li>• Corrected Vibration specification</li><li>• Corrected drive weight</li><li>• Updated Command and Register names to match ATA (drive -&gt; device)</li><li>• Updated power consumption specification.</li><li>• Added Execute SMART Function command. Also updated Command Register table (end of Ch 6 and Error Table (Ch 8) to include command.</li><li>• Reformatted Table in Ch 8 and updated description.</li></ul>	6/95